Master's thesis

A Smart Battery Management System for Electric Vehicles using Powerline Communication

Alexander Scherer

March 31, 2013

Institute for Data Processing
Technische Universität München

Alexander Scherer. *A Smart Battery Management System for Electric Vehicles using Powerline Communication.* Master's thesis, Technische Universität München, Munich, Germany, 2013.

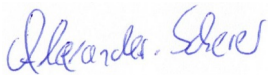
Supervised by Prof. Dr.-Ing. K. Diepold and Prof. Dr. T. Bräunl; submitted on March 31, 2013 to the Department of Electrical Engineering and Information Technology of the Technische Universität München.

Institute for Data Processing, Technische Universität München, 80290 München, Germany, http://www.ldv.ei.tum.de.

Statement

I hereby confirm that I have independently composed this Master's thesis and that no other than the indicated aid and sources have been used. This work has not been presented to any other examination board.

Munich, 31/3/13



Acknowledgements

This thesis would not have been possible without the support of many people.

I wish to thank, first and foremost, my Professor Klaus Diepold. He made me familiar with Prof. Thomas Bräunl, fundamentally helped shaping the thesis and provided me with excellent support.

I owe my deepest gratitude to Prof. Thomas Bräunl for giving me the possibility to work on such an interesting topic and for enabling my term abroad in Australia.

I would like to thank Rob Mason for the expert guidance on large battery packs and for offering his support in conducting measurements on a real-world electric vehicle.

Johannes Mühlfeld, Jeannette Bet and my parents Otto and Annette have made an invaluable contribution by iteratively discussing and proofreading my thesis.

I cannot find words to express my gratitude to my friends and family who supported me during my studies and helped me grow in so many ways.

Nomenclature

ADC	Analog/Digital Converter
BMS	Battery Management System
BPSK	Binary Phase Shift Keying
CCCV	Constant Current Constant Voltage
DoD	Degree of Discharge
ECC	Error Correction Code
EEC	Equivalent Electrical Circuit
EEEC	Electrochemical Equivalent Electrical Circuit
EIS	Electronic Impedance Spectroscopy
ESR	Equivalent Series Resistance
HF	High Frequency
IC	Integrated Circuit
OCV	Open Circuit Voltage
OPA	Operational Amplifier
PCB	Printed Circuit Board
PLC	Power Line Communication
PWM	Pulse Width Modulation
S/N	Signal to Noise Ratio
SOA	Safe Operation Area
SoC	State of Charge
SoH	State of Health
THD	Total Harmonic Distortion
UART	Universal Asynchronous Receiver/Transmitter

Summary

Background. Li-Ion cells reach an outstanding performance, but only if they are maintained well. Hence, an effective battery management system is needed to maintain a battery pack and to ensure the operation within a safe operating area. For a battery pack, this is typically done by a slave module for each battery block in series which reports cell specific information to a master device. This is in general achieved via a 1- or 2-wire connection resulting in a high installation effort, more knowledge necessary to assemble a battery pack, additional error sources and additional weight. It is examined in this work whether replacing these wires with powerline communication helps to reduce these problems.
Another issue with common battery management systems is their limited capability of obtaining deep insight into a battery's condition. This is addressed by developing on-board time-domain analysis methods.
Methods. A digital experimental verification platform is designed and assembled which is then connected to a real-world large battery pack of an electric vehicle to conduct communication reliability tests. Inner parameter estimation circuitry is developed and tested in a $LiFePO_4$ cell.
Results. Powerline communication is found to achieve a 99.9% success rate of correctly transmitted packets under the condition of an electric vehicle under load. Time-domain based inner parameter estimation can help to determine inner battery parameters.
Conclusion. Powerline communication and time-domain based inner parameter estimation are useful techniques to replace communication wires and to extend common battery management functionality from a technical point of view. These findings can help create *smart batteries* which are able to maintain themselves without the need for external devices and to communicate their state to the external device it powers by integrating the developed technology into the housing of the cells.

Contents

1 Introduction

1.1 Motivation

In a world where environmental protection and energy conservation on the one hand and the growing demand for individual transportation on the other hand are growing concerns, the development of powerful energy storage systems for electric vehicles which are both capable of providing high energy- and power densities has taken on an accelerated pace.

Lithium-ion based batteries which are known to possess the highest-in-class energy- and power density, a coulomb efficiency close to 100%, good cycle durability, low self-discharge rates and no memory effect are seen as the most promising battery technology for the next years.

However, Li-ion batteries need a relatively high maintenance effort, which even increases if multiple cells are assembled in series in order to achieve greater pack voltages which are necessary e.g. in electric vehicles. The battery management system's dual task is to prevent operation outside each cell's safe operating area and to balance cells to maximize storage capacity of the battery pack.

Reporting monitored data demands a means of communication. So far, this has been solved by 1- or 2-wire communication solutions predominantly.

This work's intention is to explore to what extend it is possible to omit these wires and replace them with powerline communication (PLC) in order to save weight and reduce wiring complexity and to implement intrinsically safe, self-managing large Li-ion battery packs.

With the Renewable Energy Project[1], the Robotics & Automation Lab of The University of Western Australia (UWA) makes a great effort to demonstrate that sustainable transportation for everybody can be carried out. Students have converted three road-going petrol cars into electric vehicles and participate at Formula SAE, an international competition for university students to design and race Formula style vehicles. Having been powered by combustion engines originally, a new category was introduced for electric vehicles in 2008 and UWA as one of the first universities takes on the challenge to rely on electric instead of combustion engines.

Contributing to this project, this thesis offers a first step towards the ultimate goal by designing a microprocessor based powerline communicating battery management system circuitry which also meets the Formula SAE rules to allow for testing under race conditions.

[1] http://www.therevproject.com

1.2 State of the Art

A state-of-the-art commercially available distributed BMS comes in a configuration identical or similar to the topology stated in figure 1.1. A so-called cell-board (CB, Slave) is connected in parallel to each cell block, measures cell parameters which are crucial for a safe operation of the block and sends the results to a so-called master module (shown in the figure as interface "BMS IN" and "BMS OUT", respectively). Popular commercial BMS using this topology include the *Lithiumate Lite* of the US-based company *Elithion* (4-wire digital solution) and the *BMS-CM100-160* of the Australian-based company *EV Power* (1-wire analog solution).

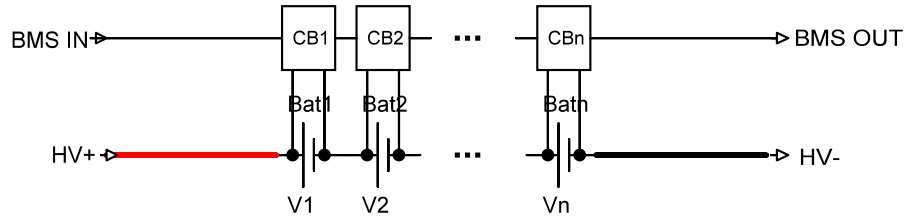


Figure 1.1: A typical battery box, consisting of multiple battery blocks in series, resulting in the high voltage terminals "HV+" and "HV-". Each block is being monitored by a cell board (CB), which communicates via a daisy-chained connector to "BMS IN" and "BMS OUT".

This approach, although logical, straight-forward and prone to electrical interference, has major disadvantages:

- Cabling complexity increases, especially with large Li-ion battery packs,
- Connectors are prone to becoming loose,
- Difficult automation, since the geometrically seperated battery wires cannot be replaced by a printed circuit board,

- Cells cannot be made intrinsically safe, as the cell-boards cannot be integrated into the battery.

The ultimate goal of easy-to-assemble, intrinsically safe battery packs is still hampered by the disadvantages listed. If there were a possibility to abolish the communication wires without losing the ability to communicate, this technology gap could be closed.

An ideal concept to overcome all detriments at once would be Powerline Communication. However, it comes along with its own challenges. The power line channel is a harsh and noisy transmission medium which is very difficult to model. It is frequency-selective, impaired by colored background noise and also affected by periodic and aperiodic impulse noise (Dostert, 2012), (Biglieri, 2003). The powerline channel is also time-varying, i.e. the channel transfer function may vary abruptly when the topology changes, that is, when devices are switched on or off. A fundamental property of the powerline channel in an electric vehicle is that the time-varying behavior mentioned before is a periodically time-varying behavior, where the frequency of the variation is a multiple of the engine revolution speed. Additional challenges are due to the fact that power line cables are often unshielded and thus become "both a source and a victim of electromagnetic interference" and must therefore include "mechanisms to ensure successful coexistence with wireless [...] systems", as well as "be robust with respect to impulse noise and narrow band interference" (Galli and Logvinov, 2008). Also, the low resistance of battery packs which can fall below $1 m\Omega$, can make transmission a challenge.

"Interest has mostly been directed toward using AC power lines to promote communication between appliances, computers and equipment within and between buildings. Less attention has been directed toward DC power lines, which are used in vehicles", Yair Maryanka, inventor of the US patent "Signaling over noisy channels", (Maryanka, 2006), granted in May 2006, formulated and took action to adapt schemes to DC power lines. From former research activities, represented in another patent (Maryanka, 1998), which deals with "high-speed transmission of data over DC power lines with error control by means of channel coding and modulation", he invented the microchip SIG60, which is further examined and used in this thesis.

1.3 Problem Statement

Several steps are taken to analyze the viability of Powerline Communications in Battery Management Systems.

First, a general description of Li-Ion batteries and their properties is given with focus on their electrical behavior.

Next, the functionality of a battery management system will be discussed in detail and possible functional impairments due to the restricted number of connectors with the PLC solution will be outlined.

Subsequently, a powerline communication solution is characterized and fitted to work

with a typical Li-Ion Battery Pack as used in electric vehicles. Requirements of a test platform are defined and the findings are transferred into a hardware design.

Three prototypes of the resulting BMS Slaves are manufactured and assembled. A firmware, offering a basic set of console instructions for access through a serial PC interface is developed.

The three developed slaves are applied in a 2-cell $LiFePO_4$ battery setup with two slaves acting as slave modules and one slave acting as the master module, as shown in figure 1.2. A successful function of this setup proves the general viability of powerline communication for battery management applications.

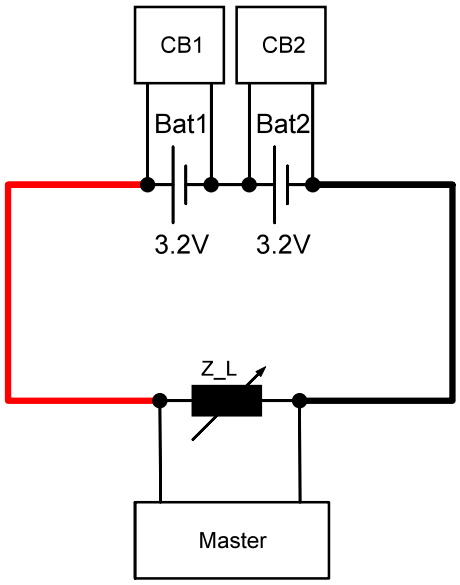


Figure 1.2: Two-cell setup. Two prototype boards work as slaves (CB1 and CB2) while the other one works as the master, proving that an effective battery management system using the battery poles only is feasible.

To face the problem of insufficient knowledge about the battery internal parameters, circuitries to achieve electrochemical impedance spectroscopy-like results without the need for external power supplies are discussed. The most suitable solution is realized in hardware on an experimental verification platform and tested on a $LiFePO_4$ cell. The problem is solved when it is possible to determine all primary parameters for a given equivalent electrical circuit.

1.4 Research Goals

The main hypothesis being explored in this thesis is to what extend distributed Battery Management Systems can abdicate communication wires by using the battery power line as the communication medium. Open questions to be answered include:

- To what extend can cheap on-board battery-powered generic ICs replace professional self-powered Electrochemic Impedance Spectroscopy measurement devices?
- Can these additional measurements contribute to an accurate state of health estimation on cell level and can deviations in cell impedance help to develop an early-warning system of imminent faults and thus significantly improve battery pack safety?
- Is PLC a viable alternative to existing 1- and 2-wire BMS solutions?

The experimental verification platform to be built contains hardware

1. to realize an effective battery management system,
2. to realize electrochemical impedance spectroscopy-like functionality and
3. a powerline communication interface.

The largest potential application are road-going passenger automobiles of which there are currently over 700 million worldwide. However, for this project the available test vehicle and first application of the research will be a Formula SAE Electric vehicle.

1.5 Thesis Guide

The thesis is subdivided into 5 parts.

Chapter 2 deals with a characterization of Lithium Batteries from an *electrical point of view*. Basic definitions are given. Similarities and differences between several commonly used *chemistries*, their correct handling and their advantages and disadvantages for several applications are pointed out. After carving how to handle a single cell, we have a look at methods to connect many cells into a larger *battery pack*. We point out the possibilities these packs can offer but also their dangers when operating them outside their safe operation area and clearly state the essential need for a Battery Management System.

Chapter 3 focuses on *Battery Management Systems* and starts by defining their tasks. Two basic topologies (*localized* and *distributed*) are presented and compared. We will

have an in-depth look at *active* and *passive balancing* technologies and also procedures to derive *battery internal parameters*, which are typically hidden from the outside and are only accessible by destruction of the cell or by electrical measurements.

Drawing from the knowledge revised in the previous two chapters, **Chapter 4** deals with the *practical design* of our own improved Battery Management System. Focused on the improvements (Powerline communication and internal state determination), the architecture is revealed and *design decisions* made are justified.

Chapter 5 is about *test benching* the newly made BMS. Is powerline communication reliable

- for battery packs of different sizes?
- for idling as well as for driving conditions?

How accurate are inner parameter estimations? Can they be used to derive secondary parameters like State of Charge or State of Health?

Chapter 6 *concludes* the work and gives an outlook to whether it is useful to pursue the initially proposed way and which further challenges need to be faced in order to achieve the *ultimate goal*.

2 Batteries

First of all, it is important to define and understand the devices that are being used as both a means of communication and source of electricity: electrochemical cells. In this chapter, the functional principle of a galvanic cell is revised. Next, we discuss its general mode of operation with a brief look at cell chemistries and chemical reactions. Then, the charging and discharging process are examined and explained and important equations like the Butler-Volmer-equation are presented. This theoretical background will build the fundament for deriving an electrochemical equivalent electrical circuit later, which we can use to characterize a battery by measurement in the later chapters. Lithium Iron Phosphate cells are given a high priority since those are the most promising solution mostly because they yield a great performance.

2.1 Electrochemical Cell

What characterizes an electrochemical cell? In general, it is a chemical device to generate and store electricity. An electrolytic cell is shown schematically in figure 2.1. The essential components are

- a positive electrode (cathode),
- a negative electrode (anode),
- an electrolyte,
- a separator and
- a housing.

The electrodes have to be as close to each other as possible to minimize the internal resistance of the cell.

The separator is a thin, usually porous, insulating material which prevents short-circuiting of the electrodes when they come in close contact. The pores of the separator are filled with electrolyte, which is capable of conducting ions between two electrodes, but which itself is an electronic insulator. Loose electrons normally cannot pass through the electrolyte. Instead, a chemical reaction occurs at the cathode consuming electrons from the anode. Another reaction occurs at the anode, producing electrons that are eventually transferred to the cathode. As a result, a negative charge cloud develops in the electrolyte

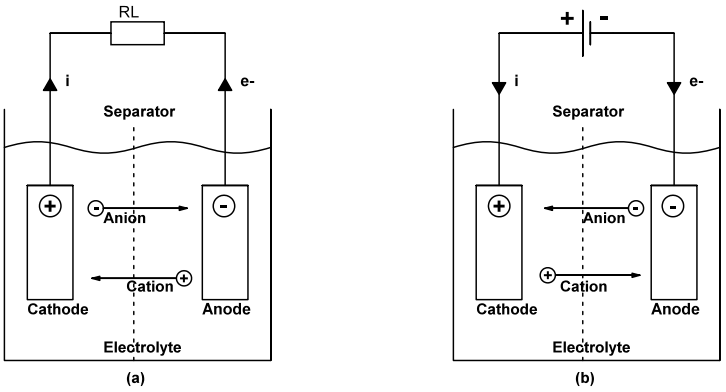


Figure 2.1: Electrochemical cell, acting as (a) galvanic cell (discharging) and (b) electrolysis cell (charging).

around the cathode, and a positive charge cloud develops around the anode. The ions in the electrolyte neutralize these charges, enabling the electrons to keep flowing and the reactions to continue. The majority of electrolytes are concentrated aqueous solutions of acids, alkalis, or salts. Through the separator filled with electrolyte, the ionic current is conveyed through the pores of the separator.

The chemical reactions which generate electricity take place at both electrodes. Each electrode undergoes a half-cell reaction. An electrode is made up of the chemicals which undergo a reaction, known as the active material (or active mass). It is attached to a metal component: the current-collector (or grid). The driving force for the external current derived from a cell is the electrode potential difference of the half-cell reactions.

An electrolytic cell which produces a current is a galvanic cell. During discharge of the cell, the current-collector of the negative electrode gathers the electrons liberated in the chemical reaction. These electrons pass through the external load and are accepted by the current-collector of the positive electrode for availability for the complementary reaction.

The chemical reactions can be written as follows.

At the negative electrode:

$$M \longrightarrow M^{n+} + ne^{-} \tag{2.1}$$

At the positive electrode:

$$nX + ne^{-} \longrightarrow nX^{-} \tag{2.2}$$

where M is a metal, X an oxidizing agent, e^{-} is an electron.

During discharging, anions move towards the anode (oxidation or anodic reaction, that means electrons are liberated) and cations move towards the cathode (reduction or cathodic reaction, with uptake of electrons) and vice versa during charging. As discharging

is the common mode of operation of a battery, the negative electrode if often known as the anode and the positive electrode as the cathode, which is the exact opposite of the convention for electrolysis. To avoid confusion, we stick with the terms of negative and positive electrodes.

Typical metals which form the negative active-mass are cadmium (Cd), lead (Pb) or lithium (Li), whereas popular positive active-mass materials are nickel (NiOOH), lead (PbO_2) and manganese (MnO_2), cobalt (CoO_2) or iron ($FePO_4$). These different possibilities for the active materials are referred to as different *cell chemistries* (Dell et al., 2001, p. 10 et. seq).

As an example of an electrochemical cell we present the $LiFePO_4$ accumulator next.

2.2 Lithium Iron Phosphate Accumulator

Two of the most promising compounds are lithium metal phosphates. Especially the olivine structured triphylite $LiFePO_4$, which was first proposed by Padhi et al. in 1997 (Padhi et al., 1997), seems suitable. Its redox potential vs. Li/Li^+ is 3.4V whereas the theoretical capacity accounts for 170mAh/g. One reason for its superior potential is that iron, the redox active species in this material, has a comparatively high Clarke number. The Clarke number is an estimation of the abundance of an element in the outermost shell of the earth. Due to its high score iron is considered to be among the five most common elements in the earth crust. In consequence, $LiFePO_4$ is a potentially low priced active material. Furthermore, it is nontoxic, environmentally benign and less prone to oxygen loss compared to other oxide based cathode materials thus ensuring high safety. Yet, $LiFePO_4$ has a major disadvantage: Its intrinsic electronic conductivity is only $10^{-9} S/cm$ (Jüstel et al., 2012). However, these properties make this type of accumulator the first choice for many electric vehicle applications. That is why we focus on this particular chemistry with the following chemical reactions involved:

Positive electrode:

$$LiFe^{(II)}PO_4 \underset{discharge}{\overset{charge}{\rightleftarrows}} Fe^{(III)}PO_4 + Li^+ + e^- \tag{2.3}$$

Negative electrode:

$$Li^+ + e^- \underset{discharge}{\overset{charge}{\rightleftarrows}} Li \tag{2.4}$$

Lithium on the one hand is extracted from $LiFePO_4$ to charge the positive electrode and on the other hand is inserted into $FePO_4$ on discharge. The standard electrode potential difference for this chemistry is $E^0 = 3.4V$. A corresponding half cell is shown in figure 2.2.

Having analysed the chemical reaction in equilibrium, we next review their behaviour while charging and discharging.

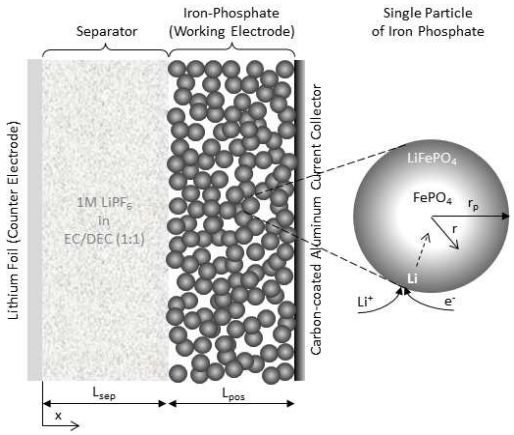


Figure 2.2: *$LiFePO_4$/Li* half-cell (COMSOL et al.).

2.3 Cell Discharging and Charging

The voltage of a cell measured under load (when drawing current) will be lower than the open circuit voltage (OCV). This results from the internal impedance of the battery which consists of:

- polarization losses at the electrodes and
- resistive (ohmic) IR losses in the grids, electrolyte and active masses.

When current flows through a battery, there is deviation from equilibrium conditions and the performance is lessbelow its maximum. The shift in potential of an electrode away from the reversible (equilibrium) value is termed the *electrode overpotential* (η). This overpotential is built up of two components:

- an *activation overpotential* caused by kinetic limitations of the charge-transfer process at the electrode. This is an intrinsic property of the electrode material immersed in the electrolyte, i.e. an interface phenomenon.
- A *concentration overpotential* which results from depletion of reactants in the proximity of the electrode due to slow diffusion from the bulk solution or across the product layer. This is an extensive property that depends on the thickness and porosity of the electrode and the ease of diffusion through it, as well as upon mass-transport processes in the electrolyte.

Taken together, these two overpotentials result in a voltage drop at the electrode during discharging, the so-called polarization loss, and the electrode is known to be polarized.

Similarly, the voltage drop due to the internal resistance of the battery is commonly referred to as resistance, ohmic polarization or overpotential.

When charging the battery, the reverse processes take place, with diffusion controlling both the macroscopic and the microscopic reaction paths within the active mass.

Polarization losses occur at each electrode and are responsible for a decreased cell voltage during discharge (V_d) and an increased cell voltage when charging (V_{ch})):

$$V_d = V_r - \eta_+ - \eta_- - IR \tag{2.5}$$

$$V_{\text{ch}} = V_r + \eta_+ + \eta_- + IR \tag{2.6}$$

where η_+ and η_- are the overpotentials at the positive and negative electrodes. This equation reduces to Ohm's Law for low overpotentials:

$$V_d = V_r - IR' \tag{2.7}$$

$$V_{\text{ch}} = V_r + IR' \tag{2.8}$$

where R' is the sum of the internal resistances of the cell and the equivalent resistances of the activation and concentration overpotentials at both electrodes. The correlation between the practical cell voltage is shown schematically in figure 2.3. An electrical equivalent circuit of the discussed resistances is given in figure 2.4 which is related to (Wenzl, 2006). In the equivalent circuit,

- $V^+ - V^-$ is the OCV,
- R_s is the resistance of the seperatar and the electrolyte,
- R_p^+ and R_p^- are the polarization overpotential impedances,
- R_{am}^+ and R_{am}^- are the resistances of the active masses of both electrodes,
- R_t^+ and R_t^- are the transition resistances,
- R_p^+ and R_p^- are the pole and grid resistances and
- R_L is the external load.

Figure 2.4 models the cell in one dimension. It is possible to extend the model to a 2D model which also takes care of the width of the electrodes but not the thickness (figure 2.5). The longer the electrode and the larger the pole resistances and currents, the higher are inhomogenities in the current.

It has been shown that the desired degree of detail is responsible for the complexity of the model used. But before deducting which model is suited best for our purposes, it is useful to learn more about how the overpotential depends on the current density of the electrodes. These correlations are defined in the Butler-Volmer- and the Nernst-Equation.

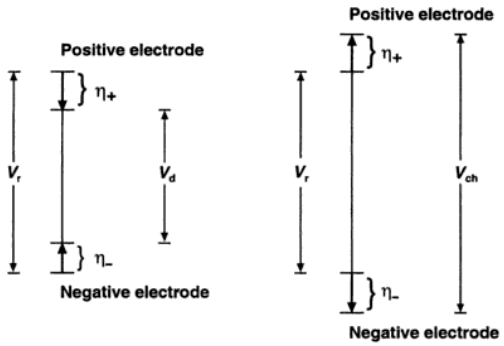


Figure 2.3: Schematic representation of the relation between practical cell voltages and reversible cell voltage (Dell et al., 2001, p. 17).

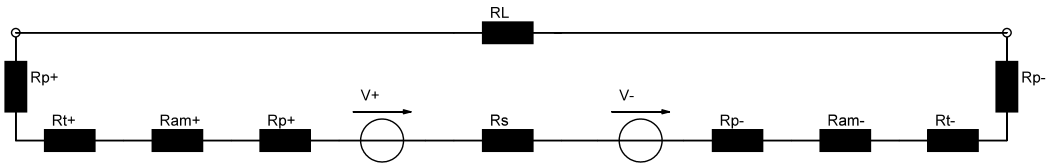


Figure 2.4: Electrical Equivalent Circuit showing the internal sources and resistances of a electrochemical cell (Wenzl, 2006).

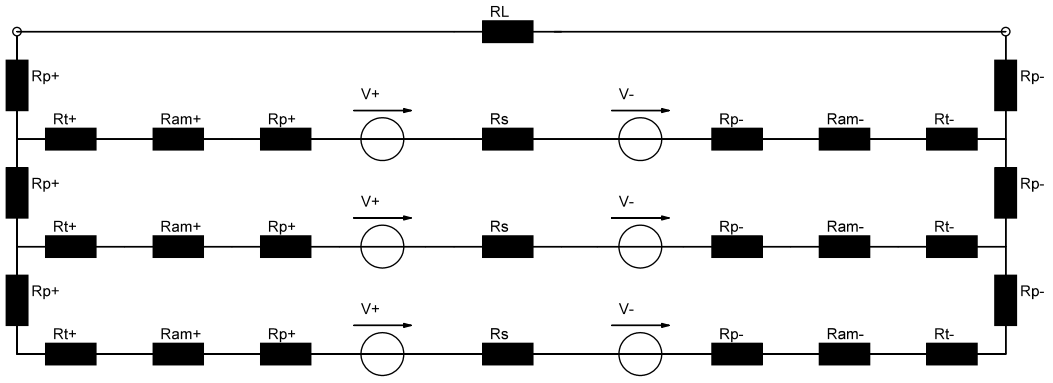


Figure 2.5: 2D Electrical Equivalent Circuit (Wenzl, 2006).

2.4 Butler-Volmer-Equation

The Butler-Volmer equation is one of the most fundamental connections in electrochemical kinetics. It describes how the electrical current on an electrode depends on the electrode potential considering that both a cathodic and an anodic reaction occur at the same electrode. It is mostly written as

$$I = A \cdot i_0 \cdot \left\{ \exp\left[\frac{\alpha_a n F}{RT}(E - E_{\text{eq}})\right] - \exp\left[-\frac{\alpha_c n F}{RT}(E - E_{\text{eq}})\right] \right\}, \tag{2.9}$$

where

- I is the electrode current [A],
- A is the electrode active surface area [m^2],
- i_0 is the exchange current density [$\frac{A}{m^2}$],
- E is the electrode potential [V],
- E_{eq} is the equilibrium potential [V],
- T is the absolute temperature [K],
- n is the number of electrons involved in the electrode reaction,
- F is the Faraday constant: $F = 9.648 \cdot 10^4 \frac{C}{mol}$,
- R is the universal gas constant: $R = 8.314 \frac{J}{K \cdot mol}$,
- α_c is the cathodic charge transfer coefficient [1] and
- α_a is the anodic charge transfer coefficient [1] (Wikipedia).

The term $\eta = E - E_{\text{eq}}$ is called activation overpotential. This overpotential depends on the electrode current. This is important because this dynamic effect can be measured and modelled.

The equilibrium potential is derived from the Nernst equation, as presented next.

2.5 Nernst-Equation

The following Nernst-Equation is used to determine equilibrium reduction potential of a half-cell in an electrochemical cell. It is also used to determine the total voltage (electromotive force) for a full electrochemical cell.

$$E_{\text{red}} = E_{\text{red}}^{-} - \frac{RT}{zF} \ln \frac{a_{\text{Red}}}{a_{\text{Ox}}} \tag{2.10}$$

as the half-cell reduction potential or

$$E_{\text{cell}} = E_{\text{cell}}^{-} - \frac{RT}{zF} \ln Q \tag{2.11}$$

as the total cell potential, where

- E_{red} is the half-cell reduction potential at the temperature of interest [V],
- E_{red}^{-} is the standard half-cell reduction potential [V],
- E_{cell} is the standard cell potential at the temperature of interest [V],
- R is the universal gas constant: $R = 8.314 \frac{J}{K \cdot mol}$,
- T is the absolute temperature [K],
- a is the chemical activity for the relevant species, where a_{Red} is the reductant and a_{Ox} is the oxidant,
- F is the Faraday constant: $F = 9.648 \cdot 10^4 \frac{C}{mol}$,
- z is the number of moles of electrons transferred in the cell reaction of half-reaction and
- Q is the reaction quotient.

The Nernst equation relates the numerical values of the concentration gradient to the electric gradient that balances it.

2.6 Equivalent Electrical Circuit

Electrical models are typically used to model

- the terminal voltage during discharging and charging,
- the terminal voltage behaviour during fast changes in current or voltage,
- to model the state of charge or state of health,
- to analyse inhomogeneities or
- to calculate temperatures (Wenzl, 2006).

Having dealt with the theoretical background of an electrochemical cell, we want create a suitable electrochemical equivalent electrical circuit (EEEC or EEC) . Every component of a battery which is crucial for the electrical properties, like electrical conductors, active masses, electrolytes, voltage source of boundary layers *et cetera*, are representated as a component of the equivalent circuit.

As we have seen in section 2.3 and in figure 2.5, the terminal voltage of a cell consists of the open circuit voltage, IR-drops over ohmic resistances and overpotentials which rise or decay exponentially over time. A still remaining task is modelling an ohmic resistance and the overpotentials η.

Every exponential transient or diffusion process, which leads to a time-shifted change in voltage after a current jump can be modelled through one or more RC elements in the equivalent circuit.

Warburg impedances (figure 2.6) demonstrates the correct way of modelling a chain of RC elements which are also used to model the capacity of long distance high voltage power lines and in general batteries where they show a similar behaviour when considering the spatial geometry of batteries (see figure 2.5).

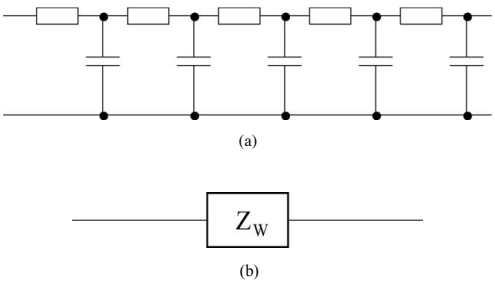


Figure 2.6: A chain of infinite RC elements in series (a) is called Warburg impedance (b) (Jossen, 2006a).

It is sufficient and common practice to model a battery as a series connection of a voltage source V_{BAT}, an ohmic resistance R_Ω, an RC element consisting of R_D and C_D to model the fast-acting diffusion overpotential (Roscher and Sauer, 2011). Another RC element consisting of R_C and C_C models the slow-acting concentration overpotential (Bhangu et al., 2005). Sometimes a series inductance L (Wenzl, 2006) is added to take care of the higher cell impedance a high-frequency signal will see. If self-discharge is considered it is possible to add a parallel resistance R_S as well (Jossen, 2006b). This set of models forms the basis for gaining a battery's internal parameters in chapter 5. The models are shown in figure 2.9.

The different approaches model the battery accomodate with the different possible types of excitation:

- The static EEC (a) sufficiently models the battery when the load attached at the terminals does not change, that is when $\frac{dI_{\text{term}}}{dt} = 0$.

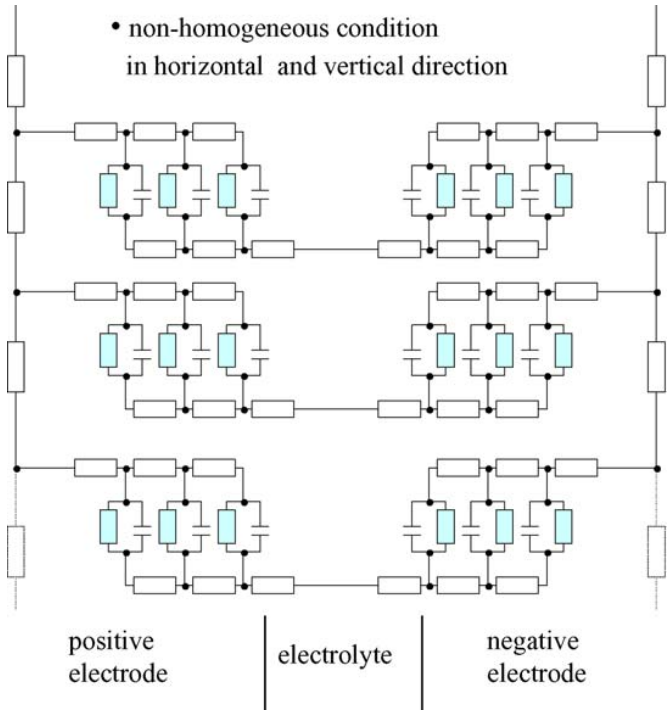


Figure 2.7: Electric equivalent circuit for a battery with porous electrodes (Jossen, 2006a).

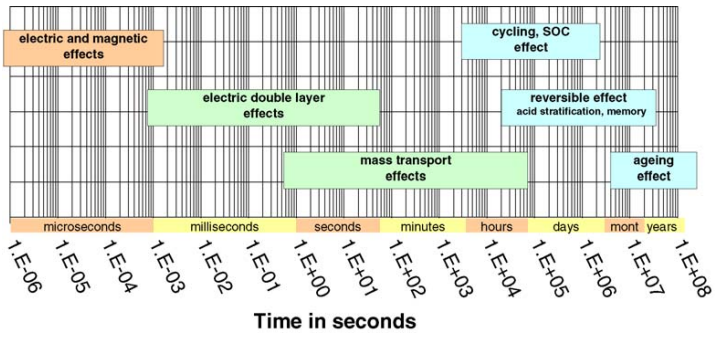


Figure 2.8: Typical time ranges of different dynamic effects of batteries. (Jossen, 2006a).

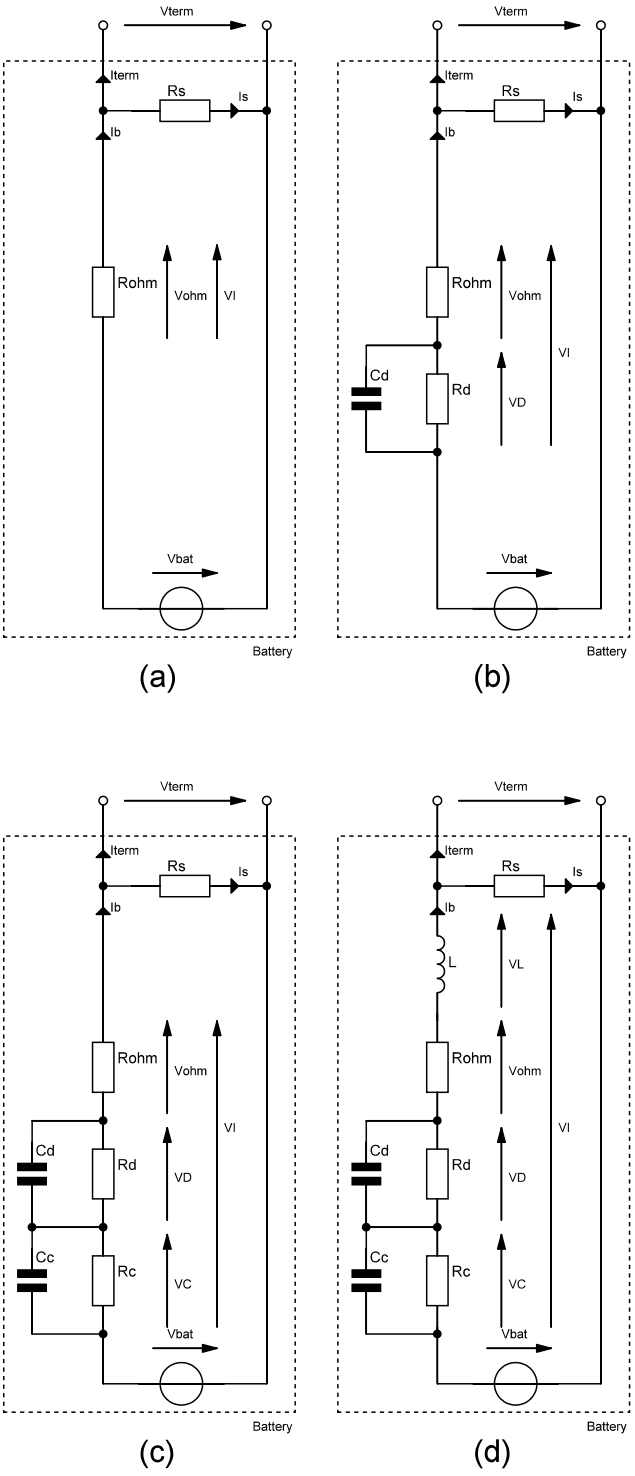


Figure 2.9: Electrochemical Equivalent Electrical Circuits. (a) Static, (b) simplified, (c) extended, (d) complete.

- The dynamic EEC in it's simplified form (b) takes into account the fast-paced diffusion overpotential process, modelled as an RC-element, which has time constants of a few milliseconds only. It needs to be taken into account for excitation frequencies > 100Hz.
- The dynamic EEC in it's extended form (c) takes into account the slow-paced concentration overpotential process, modelled as an additional RC-element with time constants in the range of several seconds or minutes, depending on the state of charge.
- The dynamic EEC in it's complete form (d) models the battery best. The series inductance models the behaviour that for very high excitation frequencies (>10kHz), the battery's impedance turns from capacitive to inductive and forms a low pass, which needs to be taken into account especially when trying to communicate over the battery.

Figure 2.10 shows an exemplary terminal voltage response when a current jump is applied, which relates to the simplified model with one RC-element.

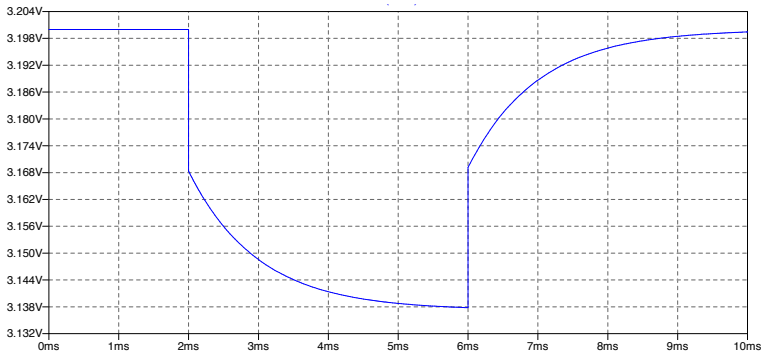


Figure 2.10: Terminal voltage of a $LiFePO_4$ cell when a load is applied. The immediate voltage drop results from the ohmic resistance, the exponential voltage drop comes from the diffusion overpotential modelling RC element.

2.7 Impedance Spectroscopy

Modelling an electrochemical system with concentrated equivalent series resistance (ESR) elements is a simplification of the complex electrochemical processes but still contains important information about the state of the cell which can be determined, if possible at all, only by destroying the cell. However, it is necessary to prove if these simplifications translate into reality.

Electrochemical Impedance Spectroscopy (EIS) is the procedure of measuring a cell's inner impedance by an external signal which consists of a range of excitation frequencies.

The results are typically plotted into a Nyquist Plot, showing the complex impedances plotted in the Gaussian plane. The result should be in line with the expected behaviour from the equivalent circuits.

Figure 2.11 shows a scientifically measured impedance spectrogram of a $LiFePO_4$ cell (Liao et al., 2005). For all measured frequencies the impedance is either ohmic or ohmic-capacitive (note that the imaginary axis shows the negative part) which reflects the behaviour expected from the derived equivalent circuits. The large semi circle (a) at low frequencies corresponds to the concentration overpotential RC element. In (b), another small semi circle at higher excitation frequencies appears which corresponds to the fast-acting diffusion overpotential RC element. An inductive part (negative imaginary resistance) can not be seen yet in these diagrams, but it is likely that the excitation frequencies were not chosen large enough.

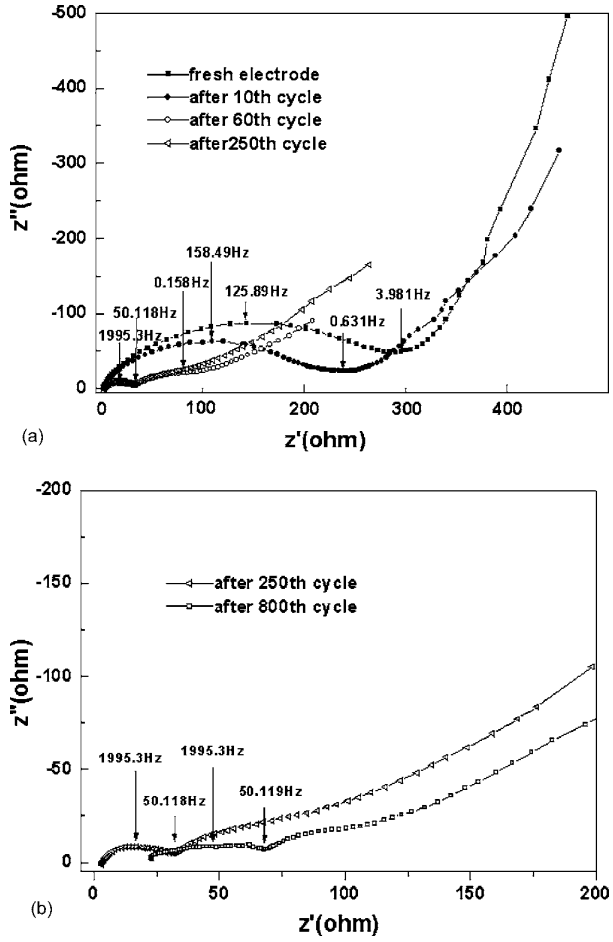


Figure 2.11: Electrochemical Impedance Spectroscopy of a $LiFePO_4/C$ cell (Liao et al., 2005).

The simplifications incorporated into the equivalent circuits proposed (replacing the Warburg impedance by only two RC elements) seems justified. It is remarked that batteries still are chemical constructions which undergo highly dynamic, non linear responses. Two EIS plots of the same battery at the same state of charge at the same temperature with the same range of frequencies but different excitation amplitudes would not provide the same results, for example. Another example is the dependancy of the capacity on the discharge current which is discussed next.

2.8 Peukert's Law

Wolfgang Peukert empirically described a dependancy between the available capacity of lead-acid batteries and the rate at which they are discharged in 1897 (Peukert, 1897). The Peukert equation is often stated as:

$$C_p = \left(\frac{I}{1A}\right)^k t \tag{2.12}$$

where:

- C_p is the capacity at a 1A-discharge-rate,
- I is the actual discharge current,
- t is the actual time to discharge the battery.

For practical cells, the capacity at a 1A discharge rate is not usually given. It is useful to reformulate the law to a known capacity and discharge rate:

$$It = C\left(\frac{C}{IH}\right)^{k-1} \tag{2.13}$$

where:

- H [h] is the rated discharge time,
- C [Ah] is the rated capacity at that discharge rate,
- I [A] is the actual discharge current,
- k [1] is the Peukert coefficient,
- t [h] is the actual time to discharge the battery

For example, a battery with a Peukert coefficient of $k = 1.2$ and a rated capacity of $C = 100Ah$ at a rated discharge time of $H = 10h$ would provide a capacity of only

$$It = 100Ah \left(\frac{100Ah}{20A \cdot 10h} \right)^{0.2} = 87Ah. \tag{2.14}$$

when discharged at $I = 20A$ and thus $t = 5h$. Peukert's law is an empirical law which is a mathematical fit of the observation with no physical background. Typical values of k are between 1.1 and 1.3 for lead-acid batteries while Lithium batteries achieve values of 1.05 and thus closer to the ideal of 1.

It is controversially discussed (Doerffel and Sharkh, 2006) whether Peukert's equation can be used to predict the SoC of a Lithium-ion battery if it is notdischarged at a constant current and a constant temperature.

2.9 Definitions and Characteristics

In the context of batteries, it is usual to use a few common definitions and abbreviations which are presented next besides typical characteristics.

2.9.1 State of Charge

The State of Charge (SoC) is the percentage of the maximum possible charge that is present inside a rechargeable battery (Pop, 2008, p. 3):

$$SoC = \frac{C_{\text{avl}}}{C_{\text{full}}}. \tag{2.15}$$

When a battery is new, the full capacity equals the nominal capacity:

$$C_{\text{full}} = C_{\text{nom}}. \tag{2.16}$$

The SoC also depends on the discharge rate and the temperature.

2.9.2 Degree of Discharge

A valuable measure is the degree of discharge (DoD) [Ah]. Though related to the State of Charge, it is given as an absolute measure rather than a relative one. For example, a 100Ah battery could be at 0% SoC at a DoD=100Ah when new but reach that SoC already after DoD=75Ah due to ageing or when discharged at a higher rate than specified, as the disposable amount of charge depends on the discharge rate according to Peukert's Law which is discussed in section 2.8. Also, when discharging a battery at a lower rate than specified, it is possible that the DoD overtops the nominal capacity C_{nom} but the initial SoC would still be 100%.

2.9.3 State of Health

State of Health (SoH) is a 'measure', typically a number between 0 and 1, that reflects the general condition of a battery and its ability to deliver the specified performance in comparison to a fresh battery (Pop, 2008, p. 3). Common numbers SoH calculation algorithms rely on are for example the cycle count, which means how often a cell has been charged/discharged, tracking of the inner impedance (see figure 2.12), tracking of the full capacity, numbers of operations outside a safe operational area (SOA) et cetera.

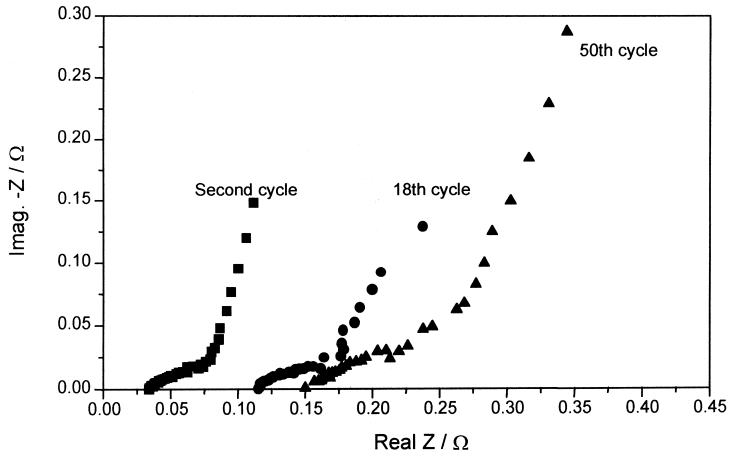


Figure 2.12: Electrochemical Impedance Spectrograms of a *NiMH* cell which suffered early damage due to a voltage decay during the initial stage of cycling (Cheng et al., 1999).

2.9.4 C-Rate

The C-Rate is a useful and commonly used nominal capacity-proportional charge- or discharge current and defined as:

$$I_C[\mathrm{A}] = C \cdot \frac{C_{\mathrm{nom}}[\mathrm{Ah}]}{1h} \tag{2.17}$$

For example, a $C_{\mathrm{nom}} = 100Ah$ battery has a 0.5C-rate of $I_{0.5} = 50A$ or a 2C-rate of $I_{2.0} = 200A$, while the discharge times are $t_{0.5} = 2h$ and $t_{2.0} = 30min$, respectively.

2.9.5 Charge- and Discharge Characteristics

Figure 2.13 shows the discharge characteristics of a $LiFePO_4$ cell at different discharge currents. Full capacity is only available at low discharge currents. However, cells which have been discharged at high rates first can be discharged at low rates to a 100% DoD.

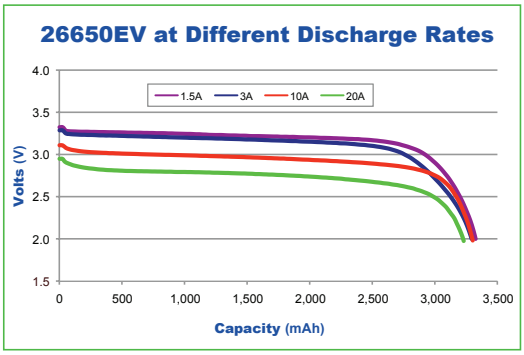


Figure 2.13: Discharge Curves of a $LiFePO_4$ cell for different discharge currents (Image courtesy of K2 Energy).

Noteworthy is the low voltage decay over large parts of the SoC. Discharge curves also reveal an internal DC resistance of approximately $20m\Omega$.

The open circuit voltage underlies a hysteresis (Roscher and Sauer, 2011), which means that the direction of previous current has an effect on the settled open circuit voltage (figure 2.14)

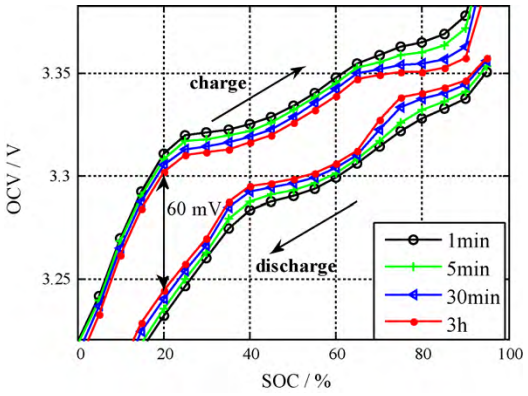


Figure 2.14: OCV curves of $LiFePO_4$-based cells depending on the previous current direction, measured after various rest periods at each step (Roscher and Sauer, 2011).

2.9.6 Temperature Characteristics

Battery behaviour is strongly dependant on the ambient temperature while - until certain limits - higher temperatures correlate with better performance. The reason for that is the *Q10 temperature coefficient*, a measure of the rate of change in a biological or chemical system as a consequence of increasing the temperature by 10°C, which is typically 2-3 in

chemical reactions. Figure 2.15 shows how the capacity of a $LiFePO_4$ cell depends on the temperature.

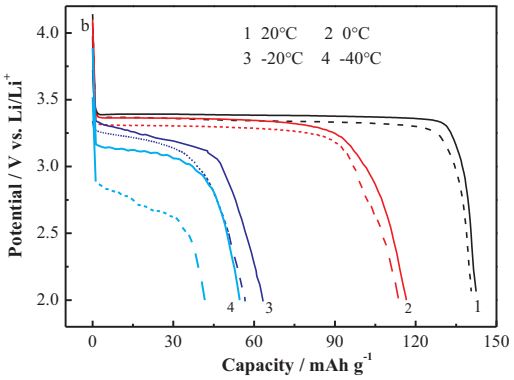


Figure 2.15: Temperature dependency of the capacity of a $LiFePO_4$ cell (Liao et al., 2012).

2.10 Chemistry Comparison

Table 2.1 compares popular cell chemistries with each other.

Benchmark	NiCd	NiMH	Lead Acid	LiCoO2	LiFePO4
Voltage [V]	1.2	1.2	2.105	3.6	3.3
Specific Energy [Wh/kg]	40-60	60-120	30-40	100-265	145
Energy Density [Wh/L]	50-150	140-300	30-40	250-730	220
Specific Power [W/kg]	150	250-1000	0.18	250-340	>300
Self Discharge Rate [%/month]	10	2-30	3-20	8	2-5
Cycle durability [1]	2000	500-1000	500-800	400-1200	more than 10000[1]
Charge/discharge efficiency [%]	70-90	66	59-92	80-90	90
Energy/consumer price [Wh/USD]	2-3	2.75	7-18	2.5	0.5-2.5
Safety	safe	safe	safe	unsafe	safe
Toxicity	highly toxic	non-toxic	toxic	non-toxic	non-toxic

Table 2.1: A small comparison of battery chemistries (Sources: Wikipedia, K2 Energy).

2.11 Battery Packs

Single cells do neither provide enough energy nor enough power for high-power applications. For this reason, they are merged into large battery packs. In that context, the following names are used for the elements a battery pack consists of:

- Cell: Basic element of a battery, providing 3V to 4V in the case of Li-Ion,
- Block: A collection of cells wired directly in parallel, providing the same voltage as a single cell,

- Battery: A collection of blocks wired in series to provide a higher voltage,
- Battery Pack: A collection of batteries, arranged in any series or parallel combination.

Picture 2.16 shows an example of a large 25.6V/128Ah $LiFePO_4$ battery consisting of 8 blocks à 40 cylindrical cells. Two of these batteries in series (yielding 51.2V/128Ah) form the traction pack of the Formula SAE car.

Dimension of one battery is 104x208x520mm. The pack can provide a continuous current of 480A and handle 30s-peaks of up to 1120A at a DC resistance of 4$m\Omega$.

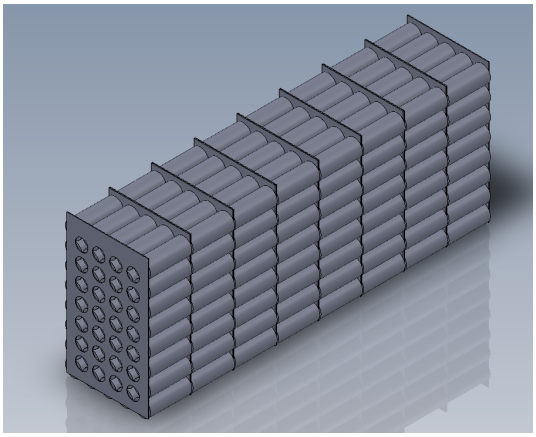


Figure 2.16: A large 25.6V/128Ah $LiFePO_4$ battery consisting of 8 blocks of 40 3.2Ah cells in parallel.

3 Battery Management System

A Battery Management System (BMS) is designed to put any of the following tasks into execution:

- Monitoring the battery status,
- Protecting the battery,
- Estimating the battery's state,
- Maximizing the performance of the battery,
- Reporting back to users or external devices.

In order to fulfil these tasks, it must accomplish the following functions:

- Prevent that the voltage of any cell exceeds a certain limit or drops below a certain limit by disabling the charging current or requesting that it be stopped.
- Avoid cell temperatures that exceed a limit by stopping the battery current directly, requesting that it be stopped, or requesting cooling.
- Prevent the charging or discharging current from exceeding a limit.

A BMS is essential when charging a Li-Ion battery. As soon as any cell reaches its maximum charged voltage, the BMS must turn off the charger (see figure 3.1). Overcharging can provoke a thermal runaway which can cause a fire.

A BMS can also balance the battery in order to maximize its capacity. This can be accomplished by removing charge from the most charged cell until its voltage is low enough so that the charger can be applied again and charge the other cells. The process is repeated until all cells are at the same voltage, fully charged, which means that the pack is balanced.

Discharging a Li-Ion battery also requires a BMS. As soon as the voltage in any cell drops to a low cutoff voltage, the load is turned off by the BMS (see figure 3.2) (Andrea, 2010, p. 16).

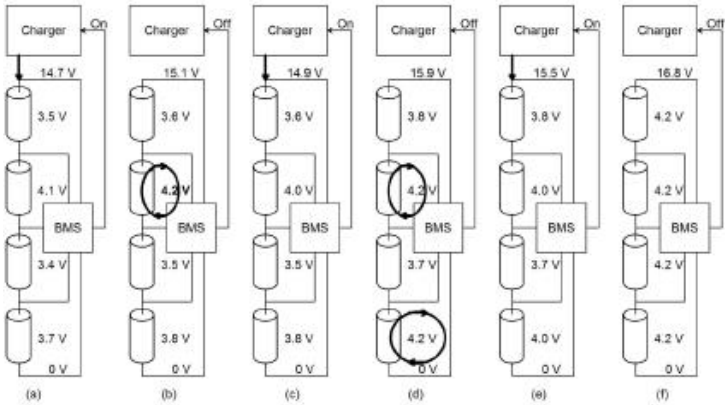


Figure 3.1: Charging with a BMS controlling the charger: (a) charging, (b) charging stops when any cell reaches the cutoff voltage, (c) charging restarts after that cell's voltage is slightly reduced by balancing and (d) the process repeats until the pack is balanced (e,f) (Andrea, 2010, p. 17).

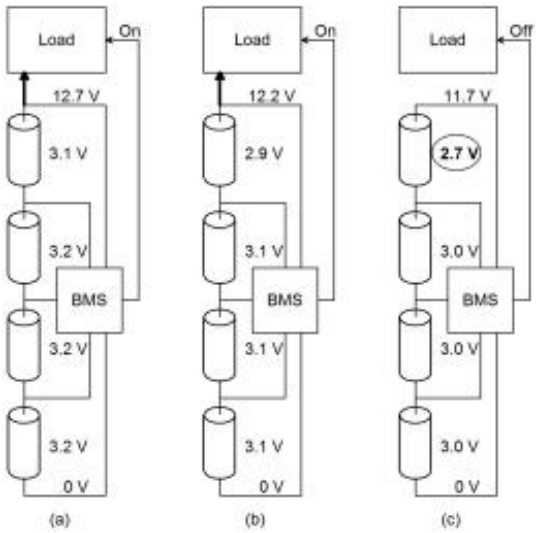


Figure 3.2: Discharging with a BMS controlling the load: (a, b) discharging and (c) discharging stops when any cell drops to the bottom cutoff voltage (Andrea, 2010, p. 17).

3.1 Topologies

How can a battery management system be realized? Three different concepts shall be compared in the next subsections, namely:

- The centralized BMS,
- the modular BMS,
- the Master-Slave-BMS,
- the distributed BMS with control wires and
- the distributed BMS without control wires (using powerline communications).

3.1.1 Centralized BMS

A centralized BMS (figure 3.3) is located in a single assembly, which is connected to the cells via a bundle of wires (N+1 wires for N cells in series). Advantages include:

- Economic reasons: only one printed circuit board (PCB) with one microchip is needed.
- Maintenance and repair: if a repair is required, it is easier to replace just a single assembly.
- Accuracy: centralized BMS use the same offsets for all cells.

Disadvantages include:

- Tap wires are referenced to high voltage and a short to the chassis results in a loss of isolation.
- "Spaghetti" problem: Hundreds of wires can run through the high voltage-section, increasing the risk of shorts considerably.
- Adding additional cells is not possible at all if all input ports are used or vice versa, some inputs might stay unused.
- No temperature measurement of each individual cell is possible.
- No voltage measurement is possible during the balancing process, as the drop in IR voltage across the long tap wire is considerably large.
- Error proneness: tap wires can fit into many inputs.
- Crimp connections are prone to getting loose.

A representative of this topology is Convert The Future's Flex BMS-48[1].

[1] http://www.convertthefuture.com/BMS.php

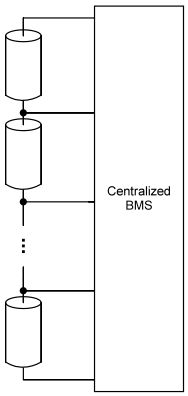


Figure 3.3: A centralized BMS architecture.

3.1.2 Modularized BMS

A modular BMS (figure 3.4) is similar to a centralized one, except it is subdivided into multiple, identical modules, each with its own wirebundle leading to one of the batteries in the pack. One module takes on the "master" role, commanding the others. Advantages include:

- Manageability: Modules can be placed close to the cells handled by it.
- Scalability: Inserting more cells is feasible by just the addition of more BMS modules.

A disadvantage is mostly the slightly higher cost, as modules have redundant functions.

3.1.3 Master-Slave BMS

In the Master-Slave architecture the functionalities are not equal as opposed to the modularized BMS. Slaves are specialized in measuring the voltage of several cells only, reporting them to a master, which has no voltage measurement function, but can communicate, calculate and control the Slaves and external protectors. Communication between master and Slaves requires a dedicated communication wire. This architecture is shown in figure 3.5. Advantages include:

- Higher specialization: more accurate voltage measurement.
- Lower costs as no unused function needs to be included in either the master or the slaves.

The main disadvantage is that a separate master and slave needs to be designed.
A prominent representative of this architecture is eLithion's Lithiumate BMS.

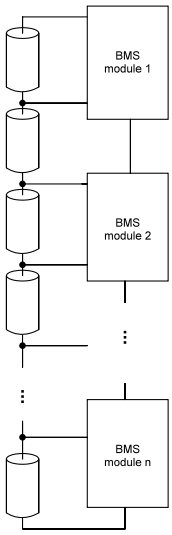


Figure 3.4: A modularized BMS architecture.

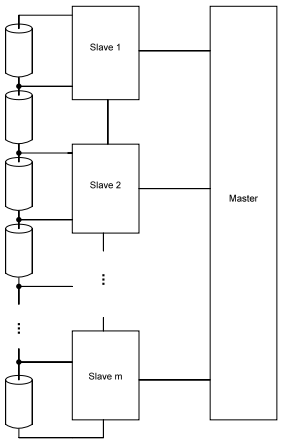


Figure 3.5: A Master-Slave BMS architecture.

3.1.4 Distributed BMS

While all the previously discussed topologies had electronics grouped and housed separately from the cells, in a distributed BMS, the electronics are contained on cell boards directly placed on the cells being monitored. There will be N modules for N cells plus one master module controlling the slaves. Communication runs over a dedicated communication wire, typically a daisy-chain connecting all slaves with the master. This solution requires 2N voltage measurement wires for N cells as well as N communication wires.

Advantages include:

- Temperature measurement of each cell is easy, as the PCB is placed right on top of the cells.
- Replacing damaged boards or cells requires detaching of only one module with two wires instead of all N+1 wires needing to be taken off when a centralized BMS fails.
- Better noise immunity due to shorter connection wires allow for more accurate voltage measurements.
- Specialization allows cheap slaves.

Disadvantages include:

- Higher costs compared to a centralized solution due to the need of N-1 additional printed circuit boards plus electronics, as well as 2N+1 more wires.
- Replacement of damaged modules can also be more difficult, as cell modules are inside the battery pack, which is sealed, when its voltage exceeds 40V.

A representative of this architecture is EVpower's ZEVA-BMS[2], which is a very minimalistic BMS. They use an analogous detection of overvoltage and a 1W passive balancing resistor on each cell, no microcontroller on the slaves and a daisy-chain where every slave can be closed (everything is okay) or open (in case of a failure). The master can then detect whether the control line is grounded or tri-state.

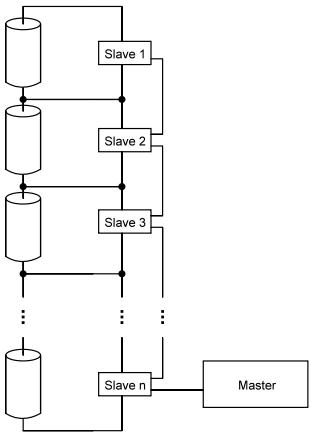


Figure 3.6: A distributed BMS architecture.

[2] http://www.ev-power.com.au/-Thundersky-Battery-Balancing-System-.html

Figure 3.7: A real-world distributed BMS setup. Image courtesy of GK Anlagetechnik.

3.1.5 Distributed BMS without communication wires

A distributed BMS without communication wires is the kind of BMS we are currently building. While the cell boards in a distributed system could theoretically even be integrated into the battery itself, as the only connections are the battery poles, the need for communication wires between the cells still exists. If it were possible to use the powerline as a communication medium, this would no longer be a hurdle. This thesis deals with the question, whether and to what extent it is possible to replace these wires by powerline communication and to create self-controlling, inherently safe cells, which is achieved by the master's ability to switch the load and the charger on and off. The topology is shown in figure 3.8.

3.1.6 Comparison

Although a centralized BMS seems to be the most logical and straightforward approach, coming at the lowest possible costs, its severe disadvantages make the use of a Master-Slave topology or a distributed topology preferable. Not only are these architectures more versatile, they also come at lower maintenance costs and maximum measurement precision without the need for "spaghetti wiring". Their main disadvantage, the expense, can still be kept low by using specialized electronics.

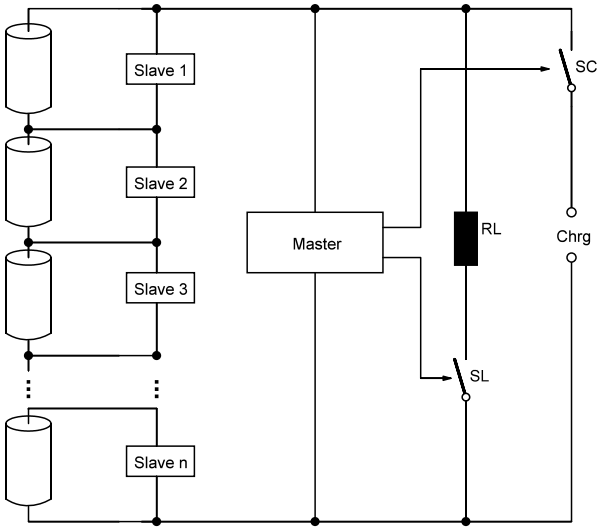


Figure 3.8: A distributed battery management system without the need for extra wiring since communication between master and slaves is established over the powerline enables the manufacturing of intelligent cells, able to report their state to an external master and receive commands, for example to balance themselves.

3.2 Measurement

3.2.1 Voltage

Measuring the voltage in each cell is crucial for ensuring operation within the safe operating area, and beyond that also essential for further determination of inner cell parameters. Whereas, in the easiest case, the cell voltage could be compared to fixed limits to prevent underdischarging and overcharging, collecting further internal parameters about the battery's state requires a more precise digital representation. The accuracy is determined by the assignment:

- Simple detection of the event of a fully charged or discharged cell requires an accuracy of no more than 100mV, since the OCV vs. SoC curve is very exact at the top and bottom ends.
- Top balancing a battery during the charging process demands an accuracy of 50mV.
- Accurate estimation of a cell's SoC from its OCV requires an accuracy of 10mV or better in order to obtain SoC estimation errors < 10%.
- Accurate estimation of a cell's SoC from its OCV in the central plateau of the OCV versus SoC curve (20% to 80% SoC) requires an accuracy of 1mV or better. This is a requirement to estimate the SoC with no knowledge of its previous history.

Resolution [bit]	Accuracy [mV]
6	62.5
8	15.6
10	3.9
12	1.0
14	0.2

Table 3.1: Required ADC resolution to achieve a certain measurement accuracy with a maximum voltage of 4V.

- To accurately estimate a cell's internal parameters without an additional amplifier, the accuracy must definitely be below 1mV, the more the better.

The accuracy requirements at a maximum voltage of 4V translates into resolution demands of the ADC, as shown in table 3.1.

3.2.2 Current

Knowledge of the battery current is necessary for the following tasks

- for Coulomb-counting fuel gauges,
- to ensure the operation within the safe operation area and
- to enable the slaves to measure the IR compensated open circuit voltage.

High currents can be measured mainly by using

- a current shunt, a small-valued, high-power and high-precision resistor (typically $50m\Omega$ or less) or
- a Hall effect current sensor

where Hall effect sensors have the following advantages

- a dissipated power of almost zero
- an inherent insulation from the pack current and
- the potential to measure the current without touching the high voltage.

The main disadvantage of Hall effect sensors is an offset at zero current, which is dependant on the temperature in addition. This could create a faultily measured SoC if based on coulomb-counting. However, Hall effect sensors are used in commercial BMS. A representative example is eLithion's Lithiumate Lite BMS. Current shunts, in contrast, have

- no offset at zero current,
- no insulation from the pack,
- a slightly variable resistance in response to temperature changes,
- introduction of quite significant energy losses (e.g. $100W$ at $100A/10m\Omega$).

Coulomb-counting demands for very high-resolution ADC because standby currents occur at levels as low as several mA. Driving currents on the other hand can reach up to $1000A$. Maxim's DS2740 Coulomb Counter features a 15-bit for currents of $\pm 5.12A$ using a $10m\Omega$ shunt, TI's BQ34Z100 fuel gauge uses a 15-bit ADC as well, gauges able to measure currents up to 9999A have been reported with 18-bit $\Sigma\Delta$-ADCs.

Figure 3.9: $1200A/50mV$ ($41.6\mu\Omega$) current shunt as sold by dutch company TBS Electronics. Image courtesy of TBS Electronics, `http://www.tbs-electronics.nl/products_batmons_acc.htm`.

3.2.3 Temperature

Measuring the ambient temperature of the battery pack is necessary. However, there is no special requirement on the accuracy - a simple thermal switch with two fixed limits is sufficient. The typical safe temperature operation range of many $LiFePO_4$ cells varies from -20 through +60 °C. Many microcontrollers come with integrated temperature sensors, which are absolutely sufficient.

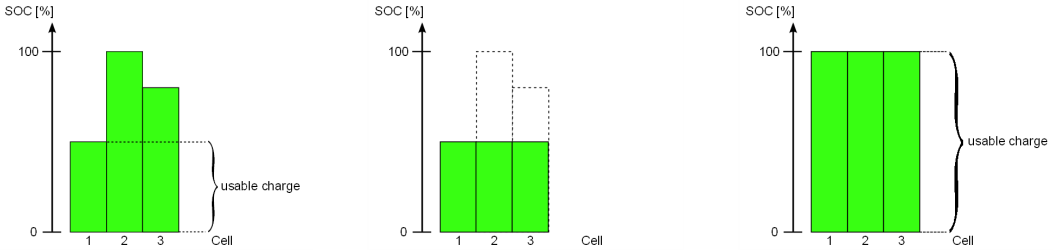
3.3 Balancing

Balancing is a very important function of every BMS to keep the amount of charge of each cell on the same level and thus maximize the available total energy of the pack. The total pack energy is limited by the block with the lowest charge. To enable the battery pack

to deliver its full energy capacity, all blocks must be able to provide the same amount of charge. When blocks are connected in series every block sees the same in- and outgoing current. Therefore, as every chain, it is as strong as its weakest link, which means in this case that the maximum amount of charge $C_{\max}$ which can be taken from or inserted into the pack consisting of n blocks with the charges C_i, $i = 1...n$ equals

$$C_{\max} = \min\{C_i\} \tag{3.1}$$

The balancing process is illustrated in figure 3.10.



(a) unbalanced (b) balancing (c) recharging

Figure 3.10: Balancing of cells with different states of charge. (a) Pack capacity is limited to weakest cell. (b) Balancing pack. (c) Full capacity available after recharging balanced pack.

3.3.1 Balancing Currents

What balancing current is needed? 100mA? 1A? 10A? The answer to this question depends on the battery size, the application and whether we talk about gross balancing or a newly installed or repaired pack or just maintenance balancing. While a 1A balancing current would balance a 100Ah pack on a rate of 1%/h and might be acceptable, it would be an overkill for a 10Ah pack. Figure 3.11 gives an overview of the time necessary to balance grossly unbalanced packs of different sizes.

In general, as soon as a pack has been balanced once, balancing only needs to equalize the different self-discharge rates. A typical self-discharge rate for $LiFePO_4$ batteries is 1%/month. Translated into a 100Ah battery, this implies an average self-discharge rate of $1.4mA$. If another cell has a self-discharge rate of $1.6mA$ the required balancing current will be only $0.2mA$, when operated continuously. However, continuous balancing is not very commonly used and thus, higher balancing currents are more common. It can be stated, though, that a 1%/h balancing current should be sufficient for most applications.

3.3.2 Algorithms

The next question arising is how to determine the amount of charge that needs to be equalized. A few promising algorithms are listed below:

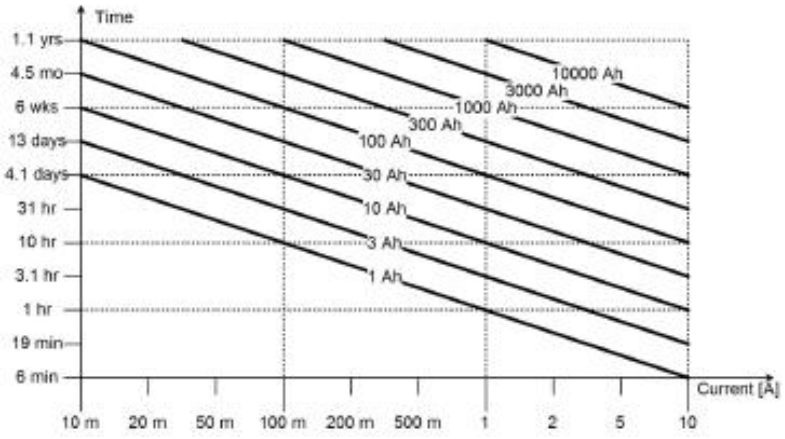


Figure 3.11: Time to balance grossly unbalanced battery packs of different capacities using different balancing currents (Andrea, 2010, p. 77).

- Voltage based algorithms,
- Final voltage based algorithms and
- SoC history based methods (Andrea, 2010, p. 66 et. seq).

The goal of each is to equalize the charge level of each cell in the pack. Voltage based algorithms aim for equalization of cell voltages, since when the voltages are equal, the SoC is equal. Balancing can take place all the time, which is an advantage, as lower balancing currents can be used. Problems with the voltage measurement occur at the flat plateau, where the OCV differences are very small, as demonstrated in figure 3.12.

This disadvantage is overcome by the final voltage based algorithm. However, it allows only a short amount of time for balancing, namely the time during which the fullest cell is in its 80%-100%-SoC area, requiring large balancing currents, which is a big disadvantage.

The SoC history based method records the SoC at the end of charge without the on-off-procedure of the charger but measures the charging current instead. As soon as any cell voltage $V_{c,i}$ starts rising quickly, the current is integrated until the last cell reaches that voltage - or until the charging process stops as the fullest cell has reached 100%. This integrated current is the charge which can be taken off that cell without risking it to fall below the SoC of the lowest cell. The balancing process can continue while idling or discharging. After a couple of recharging events, the pack is balanced, without the need for very large balancing currents or precise voltage measurement. All cells except the lowest can be balanced simultaneously.

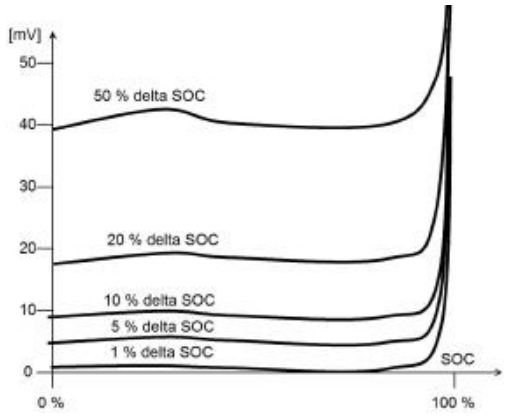


Figure 3.12: Differences in OCVs of two $LiFePO_4$ cells at different SoCs (Andrea, 2010, p. 67).

3.3.3 Top or Bottom balancing

Real battery packs consist of cells whose capacities don't match exactly. Therefore, one has to choose between equalizing the cell´s charge at the bottom and not being able to fully charge all except the lowest capacity cell (figure 3.13) or equalizing at the top, and not being able to completely discharge all cells except the one which has reached 100% first (figure 3.14).

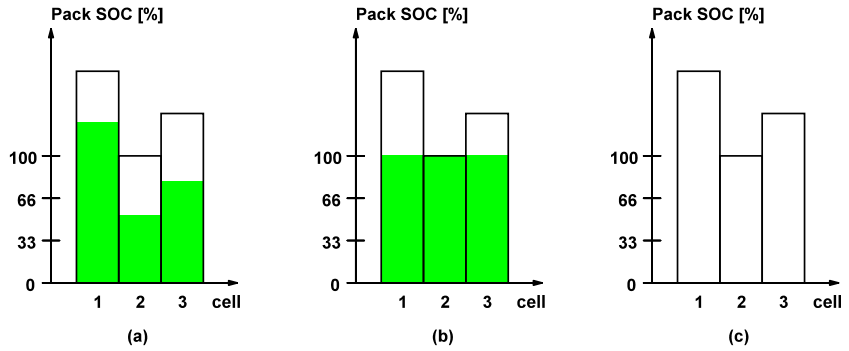


Figure 3.13: Three bottom-balanced cells of different capacities. (a) Unbalanced, (b) fully charged, (c) empty.

Which balancing method is preferable? Top balancing offers some serious advantages over bottom balancing for the following reasons:

1. *Top balanced batteries can store more energy.* Because higher SoC levels come along with higher cell voltages, the same amount of charge taken at a higher SoC level will ultimately lead to a larger energy output.

2. *Top balancing allows running of high power loads for a longer time.* That is due

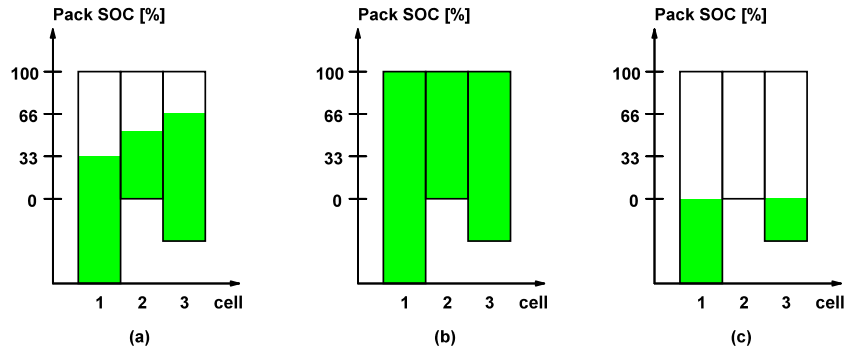


Figure 3.14: Three top-balanced cells of different capacities. (a) Unbalanced, (b) fully charged, (c) empty.

to the typically negligible low cell resistance which increases with falling SoC levels and can start limiting the maximum current drawable when many cells come close to being discharged. Since the average SoC is always higher for top balanced cells than it is for bottom balanced cells, the average total resistance is lower, too.

3. *Due to certain cell chemistries it is necessary to fully charge cells every once in a while to maintain an internal chemical balance.* For these kinds of cells, top balancing is the only considerable method.

4. *Top balancing is more accurate* if the SoC is derived from the terminal voltage. IR drops turn out to be lower at lower currents and the charging current is typically lower than the discharging current.

5. *Top balancing is more forgiving if the BMS is overridden.* A Li-Ion cell dies when underdischarged and therefore a BMS should be in charge of stopping the discharge when any cell is low. However, the electric car user may decide to override the BMS. If the cells are bottom balanced, all cells will start to die while only the weakest cell will die if they are top balanced.

6. *Charging top balanced cells is easy.* A CCCV charger can charge top balanced cells. Constant current is used until one cell is full. Taking a battery on and off the charger is easily feasible when the cells are top balanced. Constant voltage is applied when the current is gradually reduced, until all cells are equally charged (figure 3.15). This algorithm, though working well, has one major limitation: Balancing can only occur during a short period of time. As a consequence, this requires large balancing currents or long queue times (Andrea, 2010, p. 75 et seq.).

Balancing can be passive (energy is wasted in heat) or active (energy is transferred between cells). In the next subsections, a selection of promising techniques of both kinds are presented.

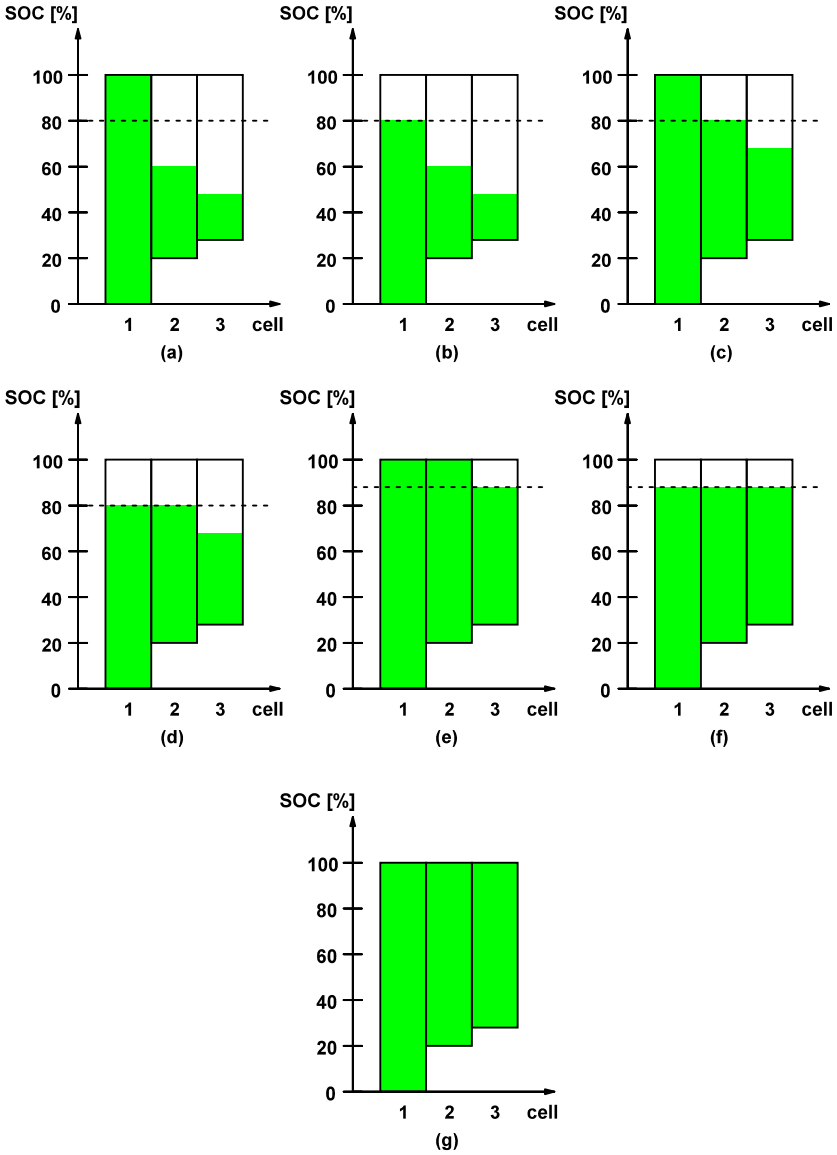


Figure 3.15: Final voltage based top balancing algorithm. After one cell is charged up to 100% SoC (a), charging is suspended by the BMS and all cells above 80% charge or more than the lowest one are balanced to 80% SoC (b, d) or until matching the lowest SoC (f), whichever occurs first. Afterwards, the charging is resumed (c, e), until all cells have reached 100% SoC (g).

3.3.4 Active Balancing

The basic idea of active balancing is to use external circuits to actively transport energy among cells in order to balance the cells. Though none of these techniques can be used in our BMS due to the requirement for no external wiring, active balancing techniques are an interesting and promising approach which is mentioned in this thesis.

In the last years many different active balancing techniques have been proposed. Sorted by energy flow, they can be grouped in three categories:

1. Cell to pack method,
2. pack to cell method and
3. cell to cell method.

The methods can also be categorized by circuit topology. Possible topologies are

1. shunting methods,
2. shuttling methods and
3. energy converter methods.

We first want to have a look at shunting solutions.

3.3.4.1 Shunting

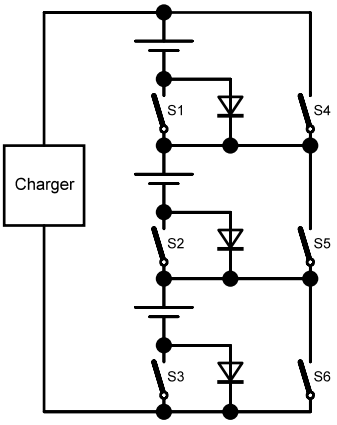


Figure 3.16: Complete shunting while charging. This method requires at least one diode per cell and two switches which need to have a resistance significantly lower than the cell itself. This is very hard to achieve especially with large batteries or at least very expensive.

Shunting techniques aim at bypassing the charging current if a cell is close to be fully charged. A complete shunting technique requires two switches and a diode per cell. The

setup is shown in figure 3.16. As an example, the top most battery has S1 closed and S4 open while being charged and S4 closed and S1 open when full. The diode prevents short-circuiting the cell. In practical application this approach will only work if the switch resistances are substantially lower than the cell resistances, which is almost impossible to achieve, especially when it comes to large cells (100Ah) with inner resistances of less than $1m\Omega$. Other than that, the in-series switches (S1, S2, S3) must be able to handle very large currents of 1000A and more in case of an EV. These would be heavy duty and very expensive contactors. In addition, in case of a failure of the controller, which closes S1 and S4 at the same time, a low-resistance short-circuit will destroy the switches, interrupting the current of the complete pack. In summary, as this solution is merely an intellectual pastime rather than a practical solution, we want to keep looking for better solutions to actively balance a battery pack.

3.3.4.2 Shuttling

"Charge shuttling cell balancing mechanisms consist of a device that removes charge from a selected cell, stores that charge, and then delivers it to another cell" (Moore and Schneider, 2001).

Flying Capacitor There are several representations of charge shuttling schemes, an interesting one being a 'flying capacitor', shown in figure 3.17a. In this method, the cell with the maximum voltage (e.g. B_1) is selected to charge the flying capacitor C. Afterwards, B_1 is disconnected again and the cell with the minimum charge (e.g. B_3) is selected. The capacitor then delivers charge ΔQ to B_3 based on the differential voltage between B_1 and B_3:

$$\Delta Q = C(V_{B1} - V_{B3}). \tag{3.2}$$

The amount of charge which can be stored in a capacitor is already low in general and becomes problematic especially when all cells are in the flat plateau of the SoC curve and thus the differential voltage is only several millivolts. A 100mV differential voltage and a 100uF capacitor assumed, the exchanged charge is $2.78 \cdot 10^{-9} Ah$ only. A high switching frequency appears to be key to make this approach work. However, it is limited by the large RC time constants formed by the flying capacitor's equivalent series resistance. The resistance of the switch (even a MOSFET has typically at least a few $100m\Omega$) and the large capacitance. For example, a $1000\mu F$ capacitor and a 1Ω resistance result in a time constant $\tau = 1ms$, limiting the switching frequency to only few 100Hz. A large (100Ah) battery pack requires a charge shuttling device with a very large capacitor with extremely large switching currents and therefore a significant amount of energy is dissipated as resistive heat in the switches and capacitor. Although contributing to balancing, this is counter productive to the idea of active balancing. However, the technique becomes more interesting when operated in the high SoC area. This will often be the case in electric vehicles, since

they will routinely be either fully charged or empty. The shuttling device can operate while charging and discharging.

A variation of that shuttling method could be a flying capacitor for every two battery cells (figure 3.17b), swapping charge from the higher charged cell to the lower charged cell. Each capacitor only needs simple controls to activate the switches.

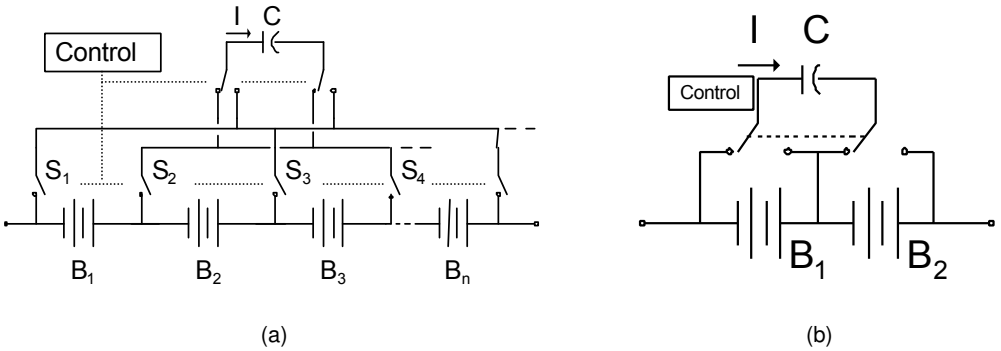


Figure 3.17: Flying capacitor charge shuttling methods for n cells, (a) using one flying capacitor, (b) using n-1 flying capacitors (Moore and Schneider, 2001).

Switched Inductor In 2000, K. Nishijima et. al (Nishijima et al., 2000) proposed a different charge shuttling method to overcome the low balancing rates of the flying capacitor. It is a pulse-width modulated (PWM) controlled balancing system, shown in figure 3.18. It uses a complimentary pair of MOSFET transistors acting as counteracting switches which are periodically opened and closed in a duty cycle proportional to the voltage difference between BC1 and BC2. In case the voltage difference is zero, the duty cycle is 50%. If BC1 has a higher SoC, the duty cycle will be shifted towards a longer closing time of S1. During this time, BC1 drives a current through S1 and L, which makes the coil build up a magnetic field and store energy in it. As the energy of a coil depends on the current according to

$$E = \frac{1}{2} L i^2 \tag{3.3}$$

and since a rapid change of energy and therefore, a rapid change of current through a coil in zero-time would require infinite power, the coil will counteract a current jump by inducing a voltage according to Faraday's law

$$V_L = -\frac{d\Phi}{dt} = -L\frac{di}{dt}. \tag{3.4}$$

This oppositely directed voltage will cause the source potential of Q2 to drop below GND and create a current over the body diode of S2, charging the battery BC2. Shortly afterwards, S2 is closed, "charging" L1 in the opposite direction, but for a shorter time interval.

The process is demonstrated graphically in figure 3.19 for better understanding. To prevent a short-circuit across both batteries when both transistors can be conductive for a short time during switching, the authors use a very short "dead time" in which both transistors are definitely open. Only the body diodes of the transistors prevent a massive voltage peak when switching.

In theory, this method, acting as a boost converter, is also able to shuttle energy from the lower charged cell to the higher charged cell, which is distinct from the flying capacitor methods.

The outstanding performancing in terms of balancing rates can be remarked in figure 3.20. The circuitry is able to transfer 325mAh of charge in less than three minutes using a switching frequency of 100kHz and a 100μH coil.

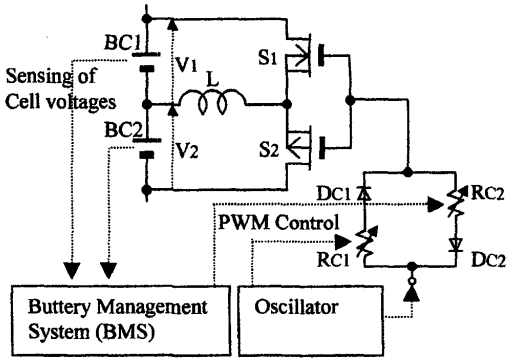


Figure 3.18: Switched Inductor Shuttling Method. Counteracting switches S1 and S2 charge the coil in duty cycles proportional to the voltage difference of two batteries BC1 and BC2 (Nishijima et al., 2000).

Active Balancing in a Modular Design

Last, this technique is examined towards it's suitability for a modular design using power line communicating slave modules. First of all, one would have to use alternating slaves with and without a coil at the negative side. Then, Slave A coil negative must be connected to Slave B positive. In this case, one loses the possibility to store the slave module inside the battery. The DC/DC converter must be able to handle voltage spikes of $2 \cdot V_{BAT} + 0.7V$. In summary, you can replace 2 transistors and two balancing resistors by 2 MOSFETs and 1 coil, saving one part, however you will need an additional bypass capacitor for powerline communications, as the coil acts as a low-pass filter, attenuating the HF signal. Gaining the ability to balance without a 100% loss in heat, we would be sacrificing the capability of a modular design towards a design of 2 batteries as the minimum entity.

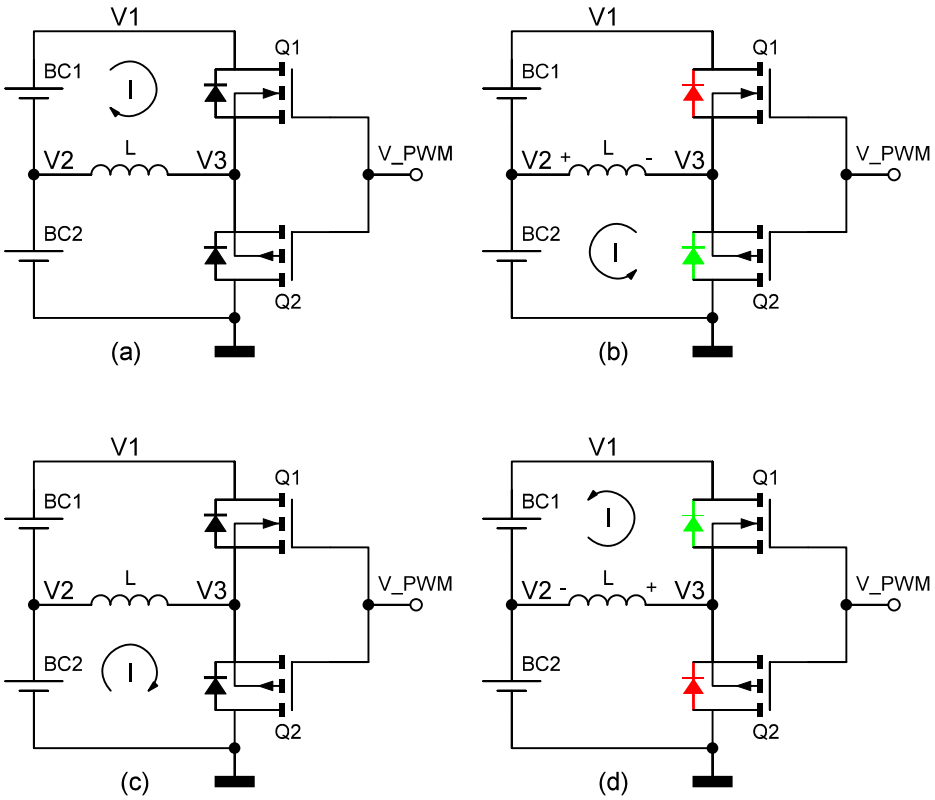


Figure 3.19: Switched Inductor Shuttling Principle. (a) V_{PWM} = high, BC1 charges L (Q1 closed, Q2 open). (b) V_{PWM} = low, Q1 opens and Q2 closes. According to the induction law L pulls V_3 below GND potential to maintain the coil current in the moment of switching and by that, it makes the body diode of Q2 conductive, thus using the lower part of the circuit to remain it's coil current. By that, it charges BC2. Q1's body diode remains non-conductive, as $V_3 < V_1$. (c) V_3 rises after L has sufficiently recovered it's energy into BC2, and the transistor Q2, which has GND potential at it's gate now, becomes conductive, as $V_{GS} < 0$. BC2 starts charging L in the opposite direction over Q2. (d) Q1 closes and Q2 opens, L forces V_3 to rise above V_1 until Q1's body diode becomes conductive and charges BC1. The duty cycle of the transistor pair's gate voltage controls which battery discharges more in average.

3.3.4.3 Energy Converters

As seen in the previous paragraph, boost converters can accelerate the balancing process. Such devices employ inductors or transformers to move energy from a cell to another or even a group of cells.

The switched transformer method (figure 3.21a) uses the same switching topology as the flying capacitor method. However, current I is taken from the entire pack and is switched into transformer T. The transformer output is rectified through diode D and delivered into cell B_n, which is determined by the setting of switches S. Electronic control selects the target cell and sets switches S. This method can rapidly balance low cells. Dis-

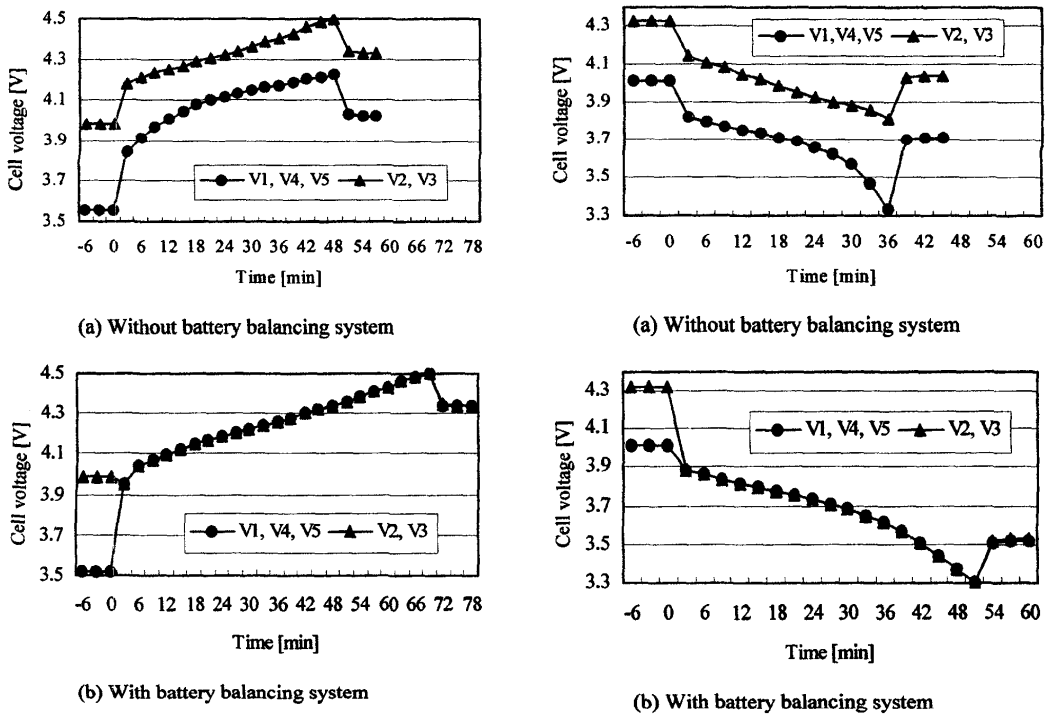


Figure 3.20: Outstanding performance of Switched Inductor Balancing both during (a) charging and (b) discharging. Five 1350mAh Li-Ion batteries, three of them empty and two of them at 50% SoC initially, are balanced after less than three minutes. (Nishijima et al., 2000).

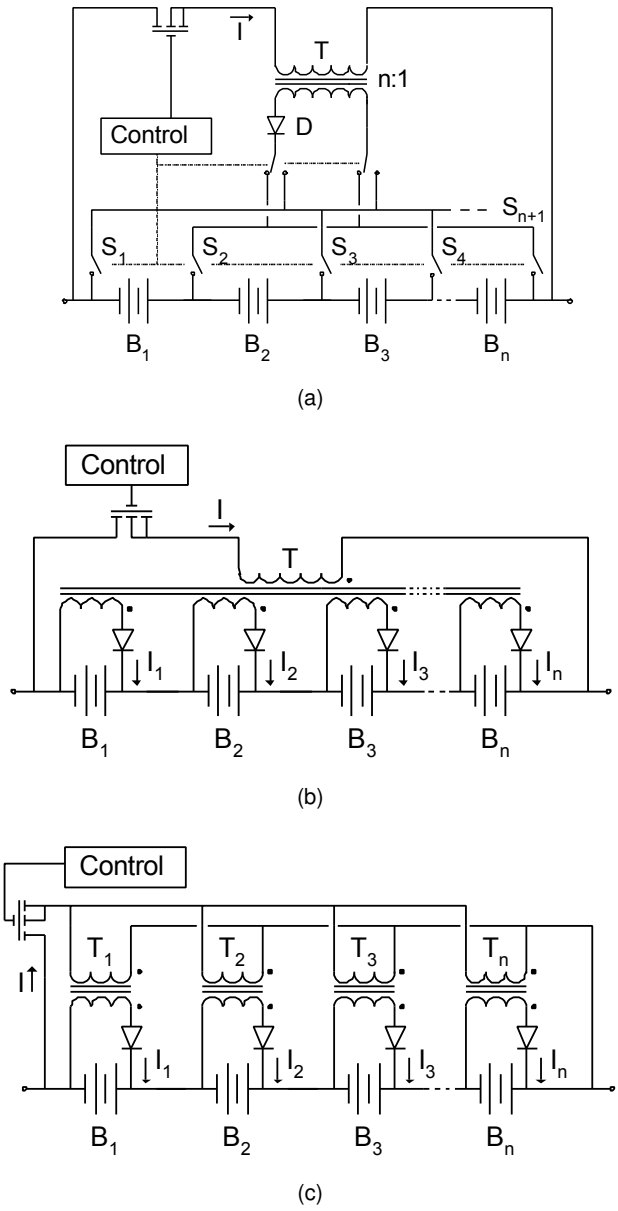


Figure 3.21: Energy Converters used for active balancing. (a) Switched Transformer, (b) Shared Transformer, (c) Multiple Transformer (Moore and Schneider, 2001).

advantages include "high complexity, high parts count in terms of control, magnetics, and switches, and low efficiency due to switching losses and magnetics losses" (Moore and Schneider, 2001).

A shared transformer is built up by a single magnetic core with secondary taps for each cell (figure 3.21b). Current I from the pack is switched into the transformer and induces currents in each of the secondaries. The secondary with the least reactance (due to a low terminal voltage on B_n) will have the most induced current. This way, each cell receives charging current inversely proportional to its relative SoC. The shared transformer can "rapidly balance a multicell pack with minimal losses" (Moore and Schneider, 2001). No closed-loop controls are required. Disadvantages are complex magnetics, a high parts count due to each secondary's rectifier and the balancing circuit being designed specifically for the given battery pack. Additional taps can not be added easily.

Using several transfomers can overcome this issue with the same result. Instead of coupling via a single magnetic core, the primary windings are coupled. This allows each cell to have its own magnetic core. Furthermore, this architecture is scalable and allows adding additional cells at a later time (Fig. 3.21c).

The shared transformer method is suitable for EV applications. If current I is designed to be small (< 100mA/Ah capacity), the device could operate "continuously at a higher efficiency than any of the other active methods" (Moore and Schneider, 2001).

3.3.5 Passive Balancing

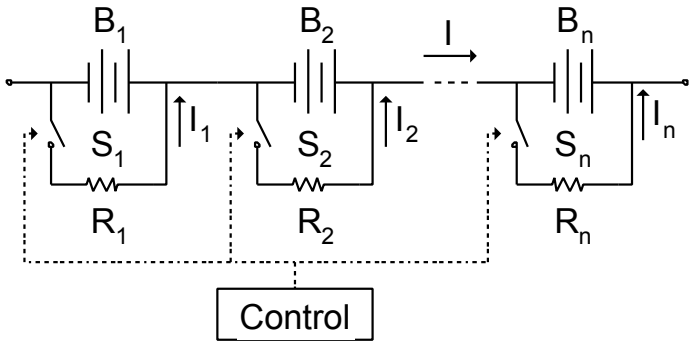


Figure 3.22: Passive cell balancing using dissipative resistors (Moore and Schneider, 2001).

Passive balancing techniques remove charge from the highest cells until they match the charge of the lowest cells. This is, in the easiest case, done by dissipative resistors which are switched by transistors operated in their active region (see figure 3.22). Although it does not seem to be a solution as elegant as the active balancing, since energy is wasted in heat, there are a lot of reasons why this technique has become the favorite of most BMS, among them:

1. Simple design.
2. Cheap parts.
3. Easy installation: no inter-cell circuitry needed.
4. Easy scalability.

Additionally, recent improvements in battery manufacturing processes have greatly minimized unbalances due to limiting different self discharge rates to a minimum level. Battery packs need to be gross balanced only after having assembled them for the very first time. After that, the balancing circuits only need to equalize tiny differences in different self-discharge rates, which are typically only a few Milliamperes in practical cells. [3]

Especially due to the constraint of having no inter-cell circuitry in our project, we rely on this solution, and design both a Bang-Bang- and a P-Balancing circuitry with adjustable balancing currents in section 4.10.

3.4 Evaluation

From the measured data, a calculation or estimation of certain parameters relating to the state of the pack may be executed by the BMS. They include

- State of Charge (SoC) and Depth of Discharge (DoD)
- Resistance and inner parameters
- Capacity and
- State of Health (SoH).

This information is not crucial for the protection of the pack, but for the convenience of the user who may be informed prior to failure, when a cell needs to be replaced or the pack needs attention.

3.4.1 State of Charge and Depth of Discharge

One thing a user is typically interested in is the battery's state of charge to estimate how much longer the battery will power their device. The flat plateaus of the SoC vs. voltage curves of lithium batteries however make fuel gauging an "inexact science" at best and a "wild guessing game" at worst (Andrea, 2010, p. 89). Almost every big chip manufacturer offers a variety of so called "fuel gauge" ICs and this subsection is dedicated to demystify their functional principle and even to coming up with a more advanced approach. While a

[3] Source: Rob Mason, Founder and CEO of Electric Vehicle conversions company EVworks `www.evworks.com.au`.

lead-acid battery's SoC can be determined by measuring the density of the electrolyte and NiCd and NiMH batteries offer steep enough SoC vs. voltage curves, a Lithium battery's SoC cannot be measured directly. However, there are multiple possibilities to estimate the SoC. Among them:

- Voltage translation,
- current integration ("Coulomb counting") and
- inner parameter translation.

3.4.1.1 Voltage Translation

State of Charge estimation by voltage translation seems easy, but is rather complicated. Figure 3.23 shows a real recorded voltage translation function of a $LiFePO_4$ cell. A 12-bit ADC with an accuracy of 1mV was used to obtain these results.

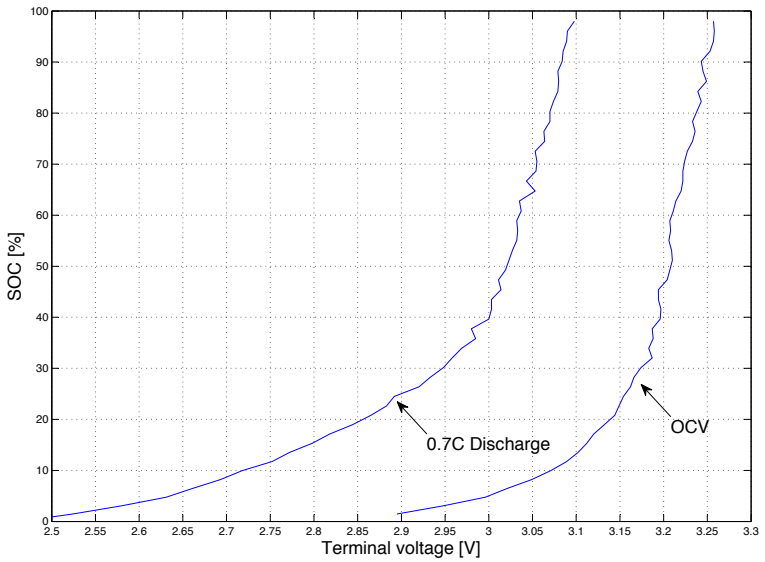


Figure 3.23: Voltage translation function obtained by a 12-bit ADC on a real $LiFePO_4$ cell.

How serious a voltage measurement error translates into a SoC estimation error is shown in figure 3.24.

Not only will

- Low-resolution ADCs

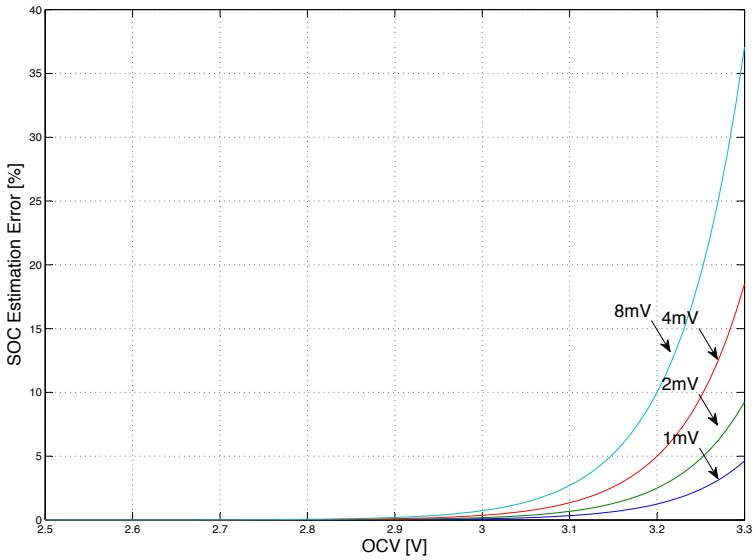


Figure 3.24: Unprecise voltage measurements lead to untolerably high SoC estimation errors. Shown are SoC estimation errors for different voltage measurement accuracies.

- variances between two different ADCs
- measurement noise and
- unprecise voltage dividers

limit the achievable accuracy massively. Variations on the cell chemistry can even shift the OCV by up to 100mV within the same $LiFePO_4$ technology.

All these limitations make an uncalibrated voltage translation the guessing game mentioned before. The BMS must at least learn the voltage transfer function for one cycle, but it is common to use voltage translation only outside the flat plateau.

3.4.1.2 Current Integration

A method widely spread is current integration or "coulomb counting". A very small-valued "shunt" resistor (typically below $10m\Omega$) is connected in series with the battery and the load. The voltage across it is proportional to the current in- or outgoing and the integration of the current is the charge taken out or put into the pack. Disadvantages include

- Cell leakage is not registered and

- offset in the measurement will result in a SoC drift.

A calibration of voltage translation at low and high SoC and coulomb counting at the flat plateau results in very good outcome.

3.4.1.3 Inner Parameters

An additional possibility to estimate the SoC without coulomb integration can be the evaluation of inner cell parameters. The feasibility will be conducted in section 3.4.3.

3.4.2 Capacity

Measuring the actual available capacity C_{avl} of a pack is required for a more accurate SoC estimation. A decrease can be used to deduct a decreased State of Health. Required for measuring the capacity is a coulomb counter and as it is possible to determine the capacity both by charging from 0% to 100% or discharging from 100% to 0%, it is preferable to do so while discharging because in electric vehicles, discharging typically happens quicker than charging and thus, the non-IR-compensated dispensable charge could be limited due to previously mentioned Peukert's law.

3.4.3 Resistance and Inner Parameters

The most sophisticated approach to gain knowledge about the battery is obtaining inner parameters and gaining further information tracking them. Inner parameters we are interested in, as shown in figure 2.9c, are:

- The ohmic resistance R_Ω,
- the diffusion overpotential parameters C_D and R_D and
- the concentration overpotential parameters C_C and R_C.

Together, those parameters form the inner resistance

$$\underline{Z} = R_\Omega + \frac{R_D}{1 + j\omega R_D C_D} + \frac{R_C}{1 + j\omega R_C C_C}. \tag{3.5}$$

The reverse evaluation can help with a better SoC determination, and tracking of these parameters can help improving the State of Health measurement.

3.4.4 State of Health

State of Health (SoH) is a 'measure' that reflects the general condition of a battery and its ability to deliver the specified performance in comparison to a fresh battery (Pop, 2008, p. 3).

The SoH indication may involve for example cycle-counting. In the simplest case the number of full charge and discharge cycles can be counted and the SoH can be calculated based of a stored maximum capacity function. For users do not always wait until a battery reaches an empty or full state the system should therefore take into account SoC levels other than empty and full. Other than that, different types of batteries and different types of user behaviour can cause problems. Due to this spread, the SoH evolution will be different for each user and application, and will consequently be rather unpredictable. It is not possible to deal with such unpredictable behaviour with a simple charge/discharge cycles counting implementation. An adaptive system must therefore be used to ensure an accurate SoC indication when the battery ages. Examples of adaptive algorithms benefit from

- Neural networks (Gérard et al., 1997), (Grewal and Grant, Oct.),
- Kalman filters (Plett, 2004) or
- Fuzzy logic (Salkind et al., 1999).

The state of health determination

- is specific for a chemistry, a type of cell, and a manufacturer
- requires a specifically fitted model derived from empirical observations and
- requires training.

Implementing, training and testing these models for specific applications and batteries is a huge task which requires expensive lab equipment, a variety of fresh batteries, programmable loads, high precision data loggers, typically 2000 charges and discharges per cell and further on. This thesis focuses on providing the hard- and firmware required to perform measurements which can then be used to train a SoH-estimation model. Ultimately, the state of health can then be used to display the remaining run-time of the battery to the user.

4 Experimental Platform

This chapter deals with the design of the experimental platform needed to meet the research goals stated in the introduction. In detail, a slave module, capable of

- measuring cell voltage,
- measuring cell impedance,
- calculating state of charge,
- calculating state of health,
- communicating with a host PC via RS232,
- communicating with other slaves via power line and
- being powered by the battery it is connected to only

with special focus on

- a small size (max. 60x75mm) to fit a standard sized 90Ah battery,
- a low price to minimize cost of the system consisting of multiple slaves and
- a low current consumption to minimize battery drain

is designed (see figure 4.1).

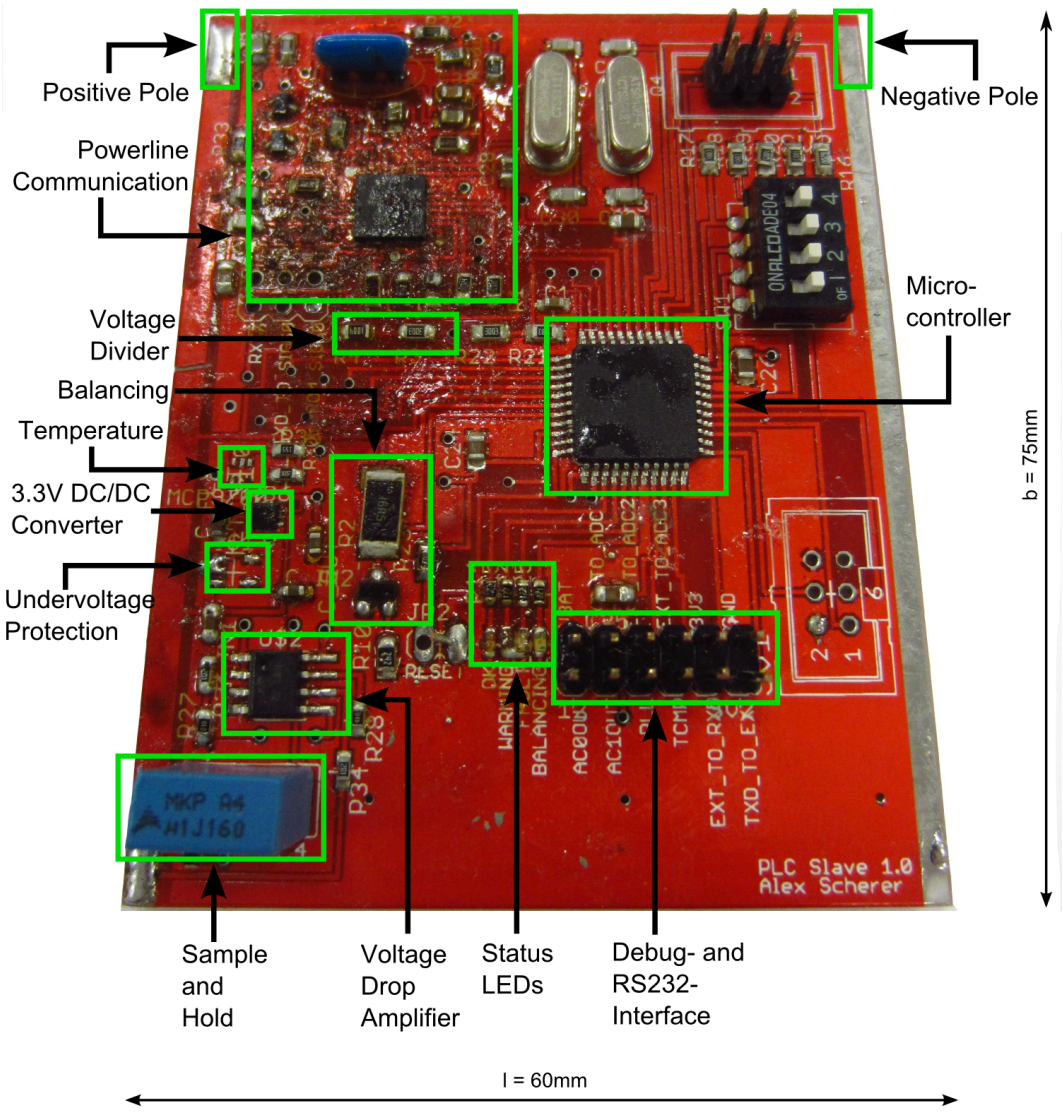


Figure 4.1: Experimental Verification Platform.

4.1 Architecture

First of all, an overview on the experimental verification platform we designed is given. Figure 4.2 shows a block diagram of the platform designed and details are discussed in the subsequent sections.

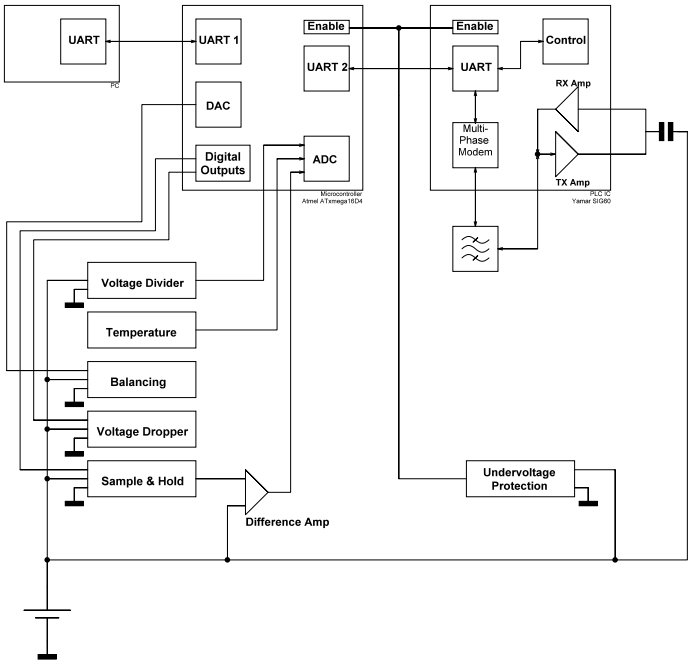


Figure 4.2: Architecture of the experimental verification platform and its interface to a PC.

4.2 Microcontroller

The microcontroller is the central unit of the slave. It communicates with the PC, executes tasks automatically, for example monitoring cell voltage and balancing, and tasks specially requested, like measuring impedance. Further, it is able to monitor data over a period of time and send it back to the PC when requested. The powerline communication IC is controlled by the microcontroller as well. There is definitely no shortage of microcontrollers. While functionalities between different manufacturers are alike, Atmel's microcontrollers stand out by offering very short execution times. Most operations are computed in one single clock cycle which helps operating them at the lowest possible clock frequency and thus, save energy. Atmel offers the very user-friendly, Visual Studio based Integrated Development Environment *Atmel Studio* and uses only one pin for programming by using

the reset signal as a clock signal during programming. The integrated on-chip debugging platform helps inspect variables and registers at runtime.

With no real constraints regarding speed and our project being far from utilising all it's plenty of features, the choice would usually have been the cheapest ATmega16 chip. Due to the need for a 12-bit Analog/Digital Converter (ADC) and the need for two Universal Asynchronous Receivers/Transmitters (UART) , one for PC communication and one for communication with the PLC Integrated Circuit (IC) , the more advanced model ATxmega16D4 is chosen in it's minimum configuration with 16kB Flash memory and 4kB boot section. Some key features contain[1]:

- Operation voltage ranging from ultra-low 1.6V to 3.6V,
- Operation frequencies of up to 32MHz,
- Ultra-low power consumption of 960µA active and 240µA idle at 2MHz clock frequency,
- One 12-channel, 12-bit, 200ksps ADC (Successive Approximation Result (SAR)),
- One 12-channel, 12-bit 200ksps DAC,
- Two Hardware UARTs,
- 16-bit real time counter,
- On-chip debugging interface,
- Sleep functionalities,
- Watchdog timer.

4.3 DC/DC Converter

We use Linear Technology's LTC3240-3.3 DC/DC Converter which is both a step up and step down charge pump, providing a stable output of 3.3V at up to 150mA. Featuring a low quiescent current of only 65µA, a shutdown current of below 1µA, high conversion efficiencies and a small package, it suits our demands very well. Important characteristics are illustrated in figure 4.3.

[1] Atmel ATxmega16D4 datasheet, `http://www.atmel.com/Images/doc8135.pdf`

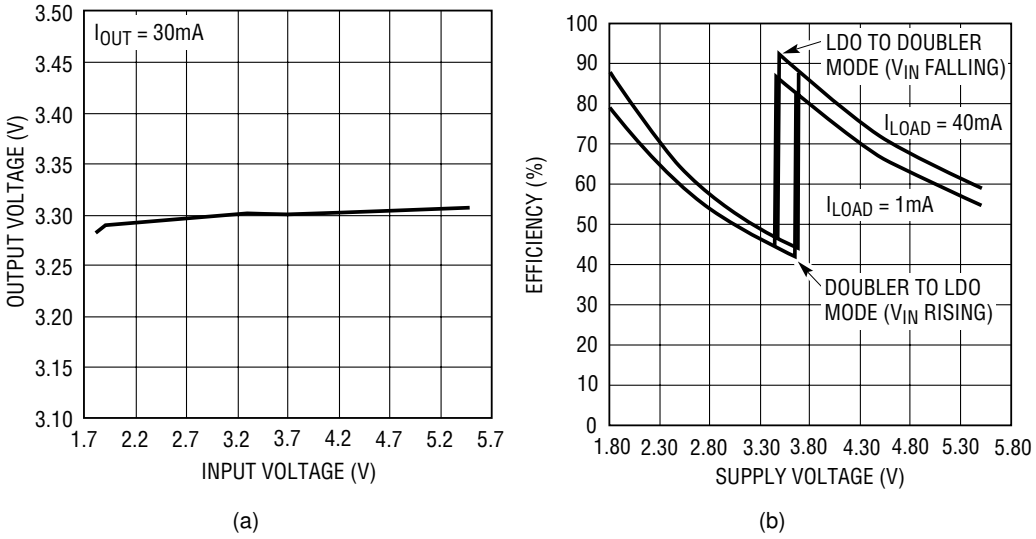


Figure 4.3: Characteristics of the LTC3240-3.3 DC/DC Converter. (a) Input-Output-Voltage-Behaviour (b) Efficiency based on input voltage. Images courtesy of Linear Technology.

4.4 Powerline Communication Device

At the moment, the only commercially available powerline communication chip optimized for battery communication is offered at an Israeli company named Yamar and is called SIG60. It provides parallel communication on 7 independant Binary Phase Shift Keying (BPSK) modulated carriers at selectable frequencies of either 1.75, 4.50, 5.50, 6.00, 6.50, 10.50 or 13.00 MHz. The message to be transmitted can be transferred via a standard serial signal consisting of one start bit (low), followed by 8 data bits and ended with one stop bit (high), at data rates of up to 115.2 kbps (at 10.50 and 13.00 MHz only). Parity check or handshaking are not supported. The device only operates at a narrow range of supply voltages of 3.0-3.6V and thus, it must rely on a DC/DC converter when battery voltages are outside of that range. The supply current is 40mA on idle and 50mA during transmission. As this is a value too high for battery applications (it would drain a 3.2Ah battery in less than 80h), the device can be set into a sleep mode where the current drain drops by three orders of magnitude to only 80µA while still being able to process messages on the powerline.

The device requires a considerably large amount of outer circuitry, which is shown in figure 4.4.

Decoded data from the powerline is output at HDO while data for transmission is accepted serially at HDI, which is being pulled high when not used by R8. Having passed the in-built multi-phase modem, the BPSK modulated signal is output through port DTxO, band-pass-filtered around the chosen carrier frequency f_c by ceramic capacitor F0 and

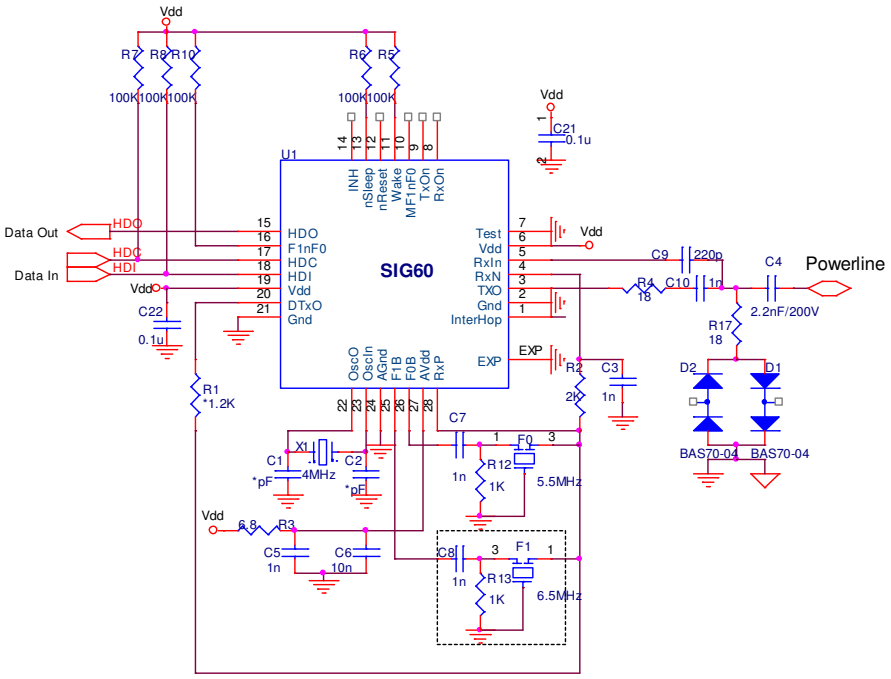


Figure 4.4: Powerline Communication IC Yamar SIG60 including outer circuitry. Image courtesy of Yamar Electronics, Ltd., `www.yamar.com/datasheet/DS-SIG60.pdf`

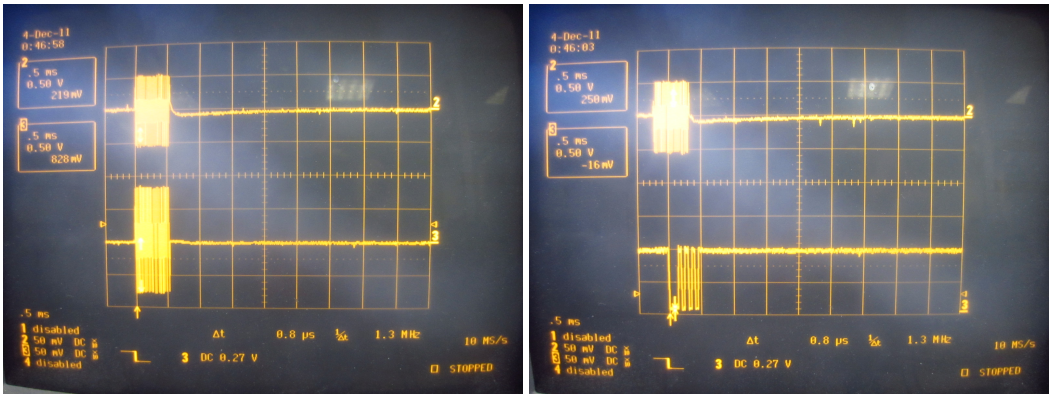
high-pass-filtered by R12 and C7 at a cutoff-frequency of 1.6kHz. After that, it is amplified by the built-in amplifier and output at TXO, where it passes the de-coupling capacitors C10 and C4 before entering the power line. The Schottky diodes D1 and D2 protect the IC from voltage spikes on the powerline. The decoding of a RX powerline signal works analogously. C5 and C6, with a piece of wire in between acting as inductor, works as a low pass filter for the voltage supply with a double pole at 22.5MHz, 5nH inductance assumed, dropping at a 40dB/dec rate for frequencies higher than the pole.

The modulated high-frequency (HF) signal and the decoded RS232-signal are shown in figure 4.5.

The subsequent sections provide insight into the communication system according to information from the patent (Maryanka, 2006) and the datasheet of the SIG60 IC.

4.4.1 Data Transmission

DC power lines are typically considered as "very noisy communication channels with high level impulse noises, causing communication errors over a wide range of frequencies. In Addition, parts of the frequencies [...] may be blocked for long periods of time as a result of Electro Magnetic Interference (EMI) or strong attenuation resulting from inter-symbol



(a) (b)

Figure 4.5: High-frequency signals on the powerline. (a) Signal attenuation: High-frequency TX (bottom) and RX (top) signal. (b) Correct decoding: High-frequency RX signal (top) and decoded byte (bottom). The signal attenuation does not depend on the distance very much, but more on capacitances parallel to the load.

interference, fading and standing waves" (Maryanka, 2006). Therefore, data is transmitted via symbol codes that have a high resistance to random errors. Resistance to errors is achieved by lengthening the symbol transmission period. According to those sources, the data which can be transmitted at data rates of up to 115.200 bauds per second or (as 2 out of 10 bauds are start and stop bits) 92.160 bits per second is translated into symbols with a symbol duration T_s of a multiple of the carrier cycle duration T_c, that is

$$T_s = n \cdot T_c, n \in \mathbb{N}. \tag{4.1}$$

The carrier frequency is

$$f_c = n \cdot f_s \tag{4.2}$$

using a symbol rate of

$$f_s = \frac{1}{T_s} \tag{4.3}$$

with n being the number of phase shifts within one symbol.

Each data symbol is a unique pattern of phase shifts, for example "+90° +90° -90° +90° -90° -90°" can represent a logical '1' and "-90° -90° +90° -90° +90° +90°" can be a logical '0' for a $n = 6$ configuration, as shown in figure 4.6[2] The receiver monitors how many phase shifts can be detected. A channel is considered bad, if more than 1 in 101 detected symbols were assigned by $m = 5 = n - 1$ detected phase shifts instead of 6. Then, the channel usage strategy is adapted, which can be:

1. Change the pattern length n,

[2]This spread spectrum technique is known from Code Division Multiple Access (CDMA), where one bit is represented by a combination of so-called "chips".

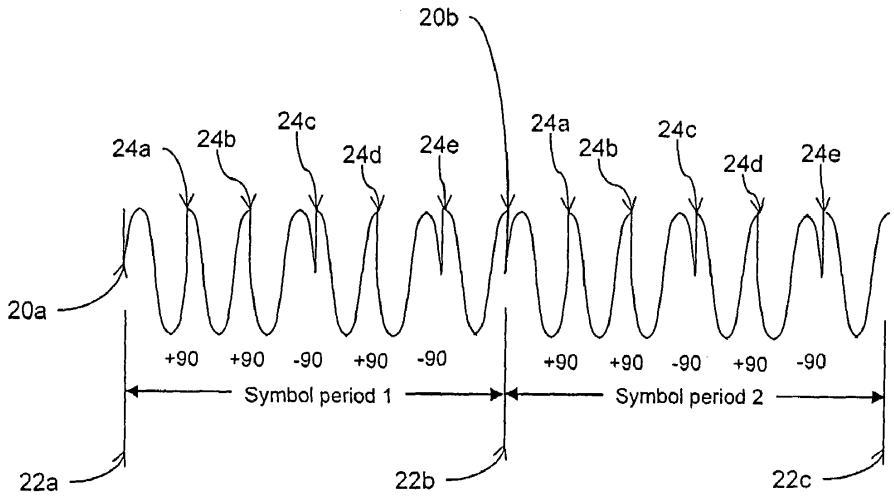


Figure 4.6: BPSK symbols used for transmission. Shown are symbols of the duration of 6 carrier cycles. 5 out of 6 phase shifts are detected by the receiver. (Maryanka, 2006)

2. Change the identification criterion, that is the needed number of correctly detected phase shifts m or

3. Cease use of a channel for communication.

Additionally, error correction codes (ECC) are used by the system, although not revealed in the patent.

Identifications can be:

1. True positive: intended pattern has been recognized correctly by the receiver.

2. False positive ("noise bytes"): Random noise on the channel causes random phase shifts of the carrier wave. A data error occurs only when noise causes a prolonged shift over most of the symbol period. Random noise is unlikely to do that for many cycles, thus the likelihood of errors decreases as the symbol period increases. That is by choosing large numbers of n at the cost of slower signaling.

3. False negative (lost signals). Can be reduced by decreasing the required number of phase shifts m.

In general, when there are serious consequences of false positive identification errors and the channel is noisy, the number of phase shifts can be increased from six to eight

and the number of detected phase shifts is increased from 5 to 6 at the cost of slower signaling (Maryanka, 2006). In the underlying system, a symbol rate of f_s = 636kHz with a symbol duration of T_S = 1.57μs, n = 6 phase shifts per symbol at a carrier frequency of f_c = 3.8MHz are used.

4.4.2 Channels

Selectable channels with their available bitrates are shown in figure 4.7.

Bit-rates				
Control_register1 (5:4)	00	01	10	11
1.75 MHz	-	-	9.6K	19.2K
4.50 MHz	38.4K	57.6K	9.6K	19.2K
5.50 MHz	38.4K	57.6K	9.6K	19.2K
6.00 MHz	38.4K	57.6K	9.6K	19.2K
6.50 MHz	38.4K	57.6K	9.6K	19.2K
10.50 MHz	38.4K	57.6K	115.2	19.2K
13.00 MHz	38.4K	57.6K	115.2	19.2K

Figure 4.7: Selectable channels with their available transmission speeds.

4.4.3 Arbitration

Since the power line is a shared medium, there must be a medium access control algorithm for collision detection and resolution to decide which device is allowed to transmit. This arbitration algorithm is shown in figure 4.8

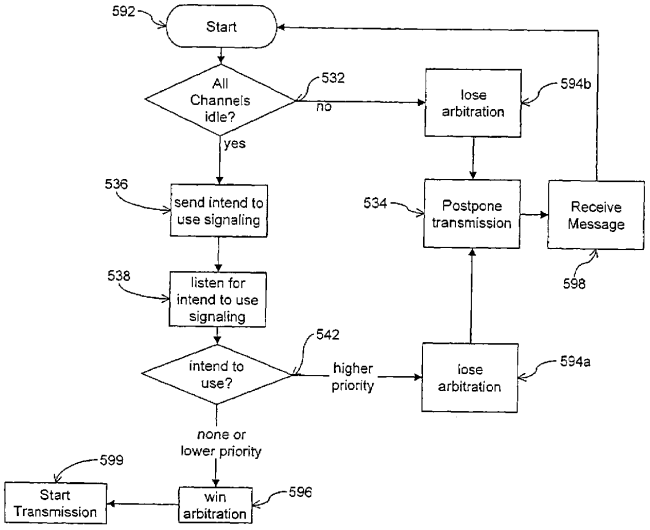


Figure 4.8: Signal arbitration algorithm used to handle multiple transmitters over a shared medium (Maryanka, 2006).

4.5 Current Measurement

Current must be known for the following reasons, as the impedance measurement requires knowledge of the actual current. Only voltage based SOC estimation is possible without knowledge of the current. But also voltage based SOC estimation methods require knowledge of the actual current, as they measure the open circuit voltage only if no current is drawn and has not been drawn for a time long enough to have the polarization effects settled. With knowledge of the current and the impedance, it will be possible to derive the SOC by the voltage only even if the current is not zero. In our test setup, the current is measured through an external in-series shunt resistor and the differential voltage applied to the ADC. In a real Battery Management System, it's the task of the master to measure the current and transmit this information to the slaves.

4.6 Undervoltage Protection

A cell specific undervoltage protector must be available to prevent the cell from being destroyed by underdischarging. For $LiFePO_4$ chemistries, the low voltage cutoff voltage is $U_{\text{min}} = 2.0V$. For that purpose, the IC LM8364-2.0 is appropriate. It draws a quiescent current of 0.65uA only and pulls the reset lines low of the other ICs on the board in case of an undervoltage condition, hence preventing them from operating and draining the battery further.

4.7 Voltage Measurement

Analog/Digital Converters have been developed and are available on the market for a very long time. Due to their popularity they exist in a vast range for almost any application, serving any demands in bandwidth, sampling time and accuracy. Our specific application has the following constraints/requirements:

1. Standby current consumption must be minimal as batteries shall maintain their charge.
2. Accuracy must be below $e \leq 1mV$ to precisely track the SOC.
3. Offset must be compensated for an offset free SOC determination.
4. Time domain measurements in the low kHz range must be possible.

Or, translated into hardware requirements,

1. both the voltage divider resistors as well as the ADC input resistance must be as high as possible,
2. the resolution must be higher or equal than $12bit$.

Offset compensation can not be performed with this architecture, the offset can be reduced to a minimum by choosing lower resistance values of the voltage divider:

$$R_2 \ll R_{\text{ADC}} \tag{4.4}$$

It is obvious that this will result in a higher standby current i. Moreover, although minimum values are typically supplied in ADC datasheets, the exact value of R_{ADC} is unknown which makes an offset free measurement more difficult. However, we will see later that it is possible to overcome this issue.

First of all, a schematic diagram of the voltage measurement circuit is shown in figure 4.9. R_1 and R_2 form a voltage divider to match the maximum input voltage of the ADC converter. Apart from the *stochastic errors*, introduced by the measurement inaccuracy of the ADC itself and inexact values of R_1 and R_2, the measurement of the true open circuit voltage V_{BAT} is superposed by the following *systematic errors*:

- *Finite resistance error*: ADC current i_{ADC}, included in i, creates a voltage drop at battery inner resistance, leading to $V_{\text{Term}} \neq V_{\text{Bat}}$.
- *ADC error*: Finite but unknown ADC input resistance $R_{\text{ADC}} < \infty$ results in an error of V_{ADC},
- *Load resistance error*: Connected loads $i_{\text{LOAD}} > 0$, which are not always avoidable, decrease V_{Term}.

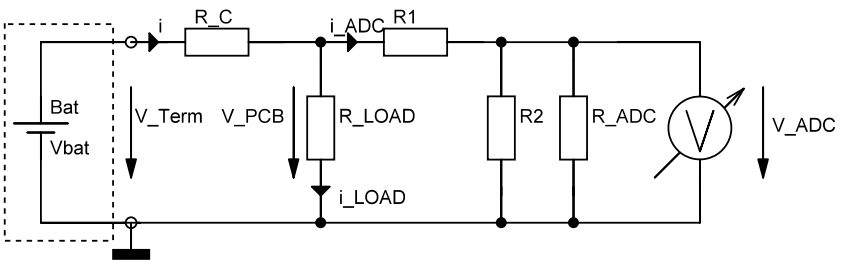


Figure 4.9: Voltage measurement setup. R_1 and R_2 form a voltage divider, R_{ADC} represents the finite ADC resistance, R_C the connection resistance and R_{LOAD} the load. The battery open circuit voltage, which is subject of interest, is V_{BAT}

.

What can be done to reduce the errors? Clearly, the stochastic errors are unavoidable and can only be minimized by choosing parts with minimal variances in their values. In terms of the systematic errors, it is obvious that the load will be connected during operation in a way that an accurate voltage measurement would depend on the exact knowledge of the battery´s inner resistance. However, in general voltage based SOC estimation while under load is not recommended. However, while not under load, only the finite resistance and the ADC error adulterate the measurement of the true open circuit voltage and both of them can be eliminated completely.

True open circuit voltage measurement

Two measurements with the same ADC but different voltage dividers allow for a true open circuit voltage measurement, as unveiled in figure 4.10 (assuming no other current is being drawn from the battery at the moment of measurement). The trick is that while the first measurement only gives a single voltage $v_{\text{ADC},1}$ corresponding to a current i_1, while the second measurement $v_{\text{ADC},2}$ at $i_2 \neq i_1$ gives the slope from which can be concluded to the open circuit voltage at $i = 0$. Although not explicitly determining the unknowns, this method eliminates the influence of all series resistances known and unknown, that is R_{ADC}, the connector resistance R_C as well as the battery´s inner resistance R_i (implicit in the battery symbol). A positive side effect is that this method works best for R_2 values of the same

magnitude order as R_{ADC}, which is in the $M\Omega$ range, and thus contributes to a low standby current usage.

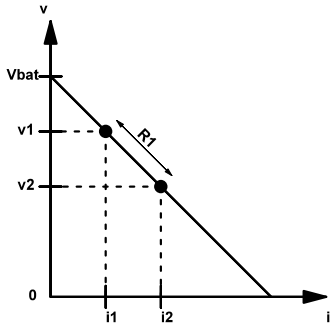


Figure 4.10: True open circuit voltage measurement principle. The OCV V_{BAT} can be derived from two measurements using different voltage divider resistors.

As shown in figure 4.11, which uses the substitutions $V = V_{\text{PCB}}$ (voltage at the printed circuit board) and $R_2 = \frac{R_1}{m}$, $m \in \mathbb{R}$, the open circuit voltage V_{Bat} can be determined by using two different values of R_1, R_{11} and R_{12}, which result in two different terminal voltages V_1 and V_2. The ADC resistance is

$$R_{\text{ADC}} = \frac{V_1 R_{11} - V_2 R_{12}}{(1+m)(V_2 - V_1)} \tag{4.5}$$

and the open circuit voltage

$$V_{\text{Bat}} = V_1 \frac{R_{11} + \frac{V_1 R_{11} - V_2 R_{12}}{(1+m)(V_2 - V_1)}(1+m)}{\frac{V_1 R_{11} - V_2 R_{12}}{(1+m)(V_2 - V_1)}}. \tag{4.6}$$

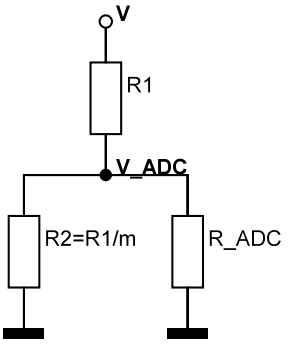


Figure 4.11: Nomenclature at the true open circuit voltage measurement.

4.8 Electrochemical Impedance Spectroscopy

Additionally to the insight into a battery's *State of Health (SOH)*, knowledge about the impedance is of great significance for the battery management system functionality:

1. *State of Health* determination is possible by tracking the complex impedance.
2. *Open Circuit Voltage* determination while charging or discharging is possible only knowing the DC resistance.

Furthermore, it can help to detect corrosion, for example at the battery poles, which can lead to an interrupted current flow in very early stages.

Electrical measurement lessons offer a variety of methods to measure the complex impedance of RLC networks. Some of the possibilities are:

1. Measurement bridge
2. Resonance method
3. I-V-method
4. Self adjusting measurement bridge method (Benger, 2007).

In general, measurements can be made in either the time- or frequency domain. Measurements in the frequency domain work in the way that an externally powered signal generator applies a sinusoidal current of varying frequencies through the battery (figure 4.12) and measures the amplitude- and phase responses to create a Bode- or Nyquist-plot with this data. The battery is the device under test, modelled as Z_{DUT}, and its values are determined by

$$\underline{Z}_{\mathrm{DUT}} = \frac{\underline{V}_{\mathrm{DUT}}}{\underline{i}} \tag{4.7}$$

where $\underline{i}$ is determined over the internal shunt resistor.

Other measurement methods can be found at (Benger, 2007).

In our setup, we want to measure these parameters without an external power supply (figure 4.13). Our DUT has the dual function of powering the AC signal generating circuit as well as being the DUT itself.

The signal generator could be realized by using the DAC of the microcontroller plus subsequent amplifier, however the linearity could be greatly affected when it comes to frequencies so high that the intended sinusoidal waveform becomes edgy. Using timers to create pulse-width modulated on/off waveforms plus subsequent analog filter bank and amplifier could reduce these problems. In any case, an amplitude detector and a phase detector is needed to calculate the complex impedance. The amplitude detector can be a peak-type rectifier and the phase detector can be realised by using a 1-bit comparator plus a fast-counting counter, both provided by the microcontroller. The fast-acting counter

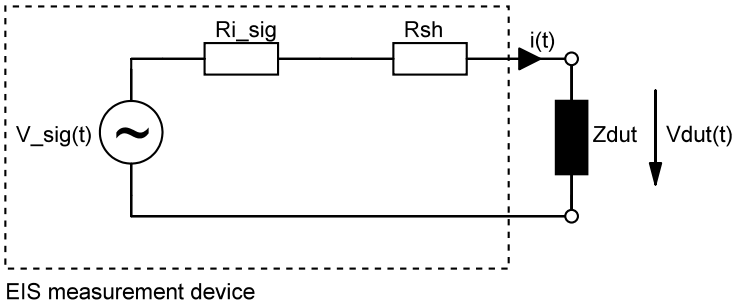


Figure 4.12: A typical I-V-measurement setup as used in many EIS measurement devices. The signal generator comes along with its own power supply.

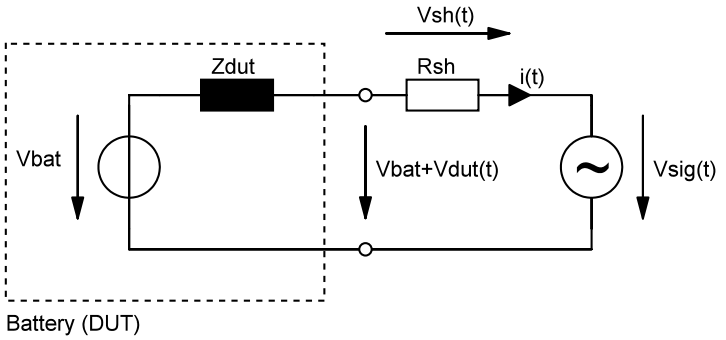


Figure 4.13: An I-V-measurement setup as used in our setup. The signal generator is powered by the DUT.

counts the ticks from when $V_{\mathrm{DUT}}(t)$ crosses zero until $i(t)$ crosses zero. This value is proportional to the phase difference.

Though a proper EIS without an external device or external power supply is conceivable, for a first approach we focus on a time-domain based measurement, leaving the option for changing towards a frequency-domain measurement if the results turn out to be insufficient. Time-domain based measurement requires less sophisticated circuitry but more complicated estimation algorithms. The next section describes the knowledge necessary to understand time-domain based impedance measurement.

4.9 Time-domain based Impedance Measurement

Measuring impedance in the time-domain relies on applying a current jump and capturing the dropping terminal voltage recovery afterwards. The amplitude of the voltage drop depends on the magnitude of the current jump and the inner cell resistance. Unfortunately, it is of advantage to use small currents (to not drain the battery) and the impedances of large traction battery blocks can be as low as several $100\mu\Omega$. This can result in voltage

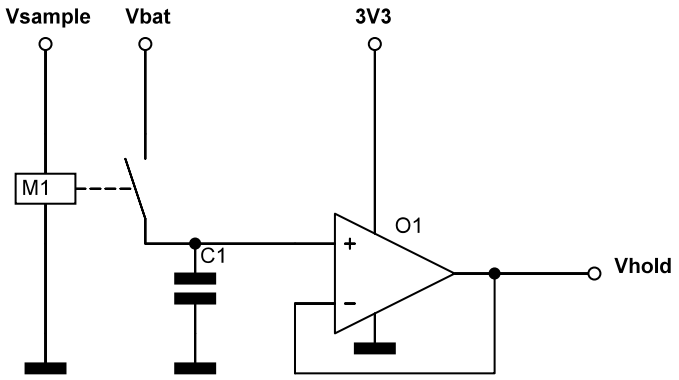


Figure 4.14: Sample and Hold circuit.

drops as low as $100\mu V$ which can not be resolved by the ADC without prior amplification. Hence, a voltage drop amplifier, capable of amplifying a differential voltage on the upper rail of the supply voltage is designed. A very low-droop, analog sample and hold-circuit holds the old voltage prior to dropping it.

4.9.1 Sample and Hold

Sample and Hold circuits are mainly characterized by their switch delay time, acquisition time to achieve an n-bit accuracy and an effect called droop and come in a large variety for many applications of interest.

The focus for our application is much more on minimizing the droop effect rather than optimizing it's acquisition time, as the time delay between sampling and dropping the battery voltage can almost be chosen arbitrarily and subsequent measurements usually are several minutes apart from each other. Droop refers to the storage capacitor's leakage of charge, which is caused by it's internal finite parallel resistance and by current flowing into the operational amplifier input due to its finite input resistance. Also a very high isolation resistance of the switch M1 is important. Figure 4.14 shows a simple sample-and-hold circuitry in accordance to (Tietze et al., 2002, p. 978 et seq.[3]).

The principle of operation is: If the relay M1 is triggered by setting high V_{sample}, the storage capacitor C1 is charged to the value of the battery voltage V_{BAT}. When C1 has been loaded sufficiently, M1 opens, such that C1 stores the old voltage. To provide this voltage

[3] In the literature, an additional input op amp is used in front of the storage capacitor to prevent putting strain on the source. As we are dealing with very low resistance batteries, the input op amp is neglectable.

R_{on}	R_{off}	V_{coil}	I_{coil}	$I_{contact}$	$t_r + t_f$
0.1Ω	$5T\Omega$	$3V$	$6mA$	$0.5A$	0.7ms

Table 4.1: Technical parameters of SIL03-1A72-71D Relay.

for subsequent usage, the operational amplifier O1 is used as an impedance converting voltage follower, providing the same voltage as on it's high-impedance input.

4.9.1.1 M1 (Switch)

M1 works as the main switch. It must be capable of providing an almost infinitely large resistance when closed to isolate the stored value from changes in the battery voltage afterwards. MOSFETs, which are typically suggested for this purpose, do not work for our intentions, as their isolation resistance of only a few $M\Omega$ would discharge the storage capacitor too quickly, as the time constants would be in the range of $\tau = 1M\Omega \cdot 100nF = 100ms$ (assumed using a DMG1013T PMOS transistor). It depends on the time required to hold the value. If we were sampling at, say, 1MHz, a MOSFET would be a suitable solution. As we need to hold the value for at least 30 seconds at a droop rate of less than several $\frac{1\mu V}{s}$, we need isolation resistances as high as several $1T\Omega$. The only device which can provide isolation resistances that large are reed relais and among them there is only one which provides the necessary $1T\Omega$ and a trigger voltage of 3.3V. Therefore, our choice is the MEDER SIL03-1A72-71D relay. Some important parameters are summarized in table 4.1.

4.9.1.2 C1 (Hold Capacitor)

The storage capacitor must

1. be large to obtain a low droop,
2. have very low self discharge and
3. have no hysteresis.

Electrolytic and aluminium capacitors, though they offer high volumetric capacitances, cannot be used due to their high self discharge and hysteresis. Also the popular small and fast ceramic capacitors cannot be used due to noteworthy hysteresis. A good choice are polypropylene capacitors, which do not show any hysteresis. On the downside they become more pricey the higher their capacitance values, which are not very high in general due to their very low volumetric capacitance. We use a $100nF$ polypropylen capacitor, which is good trade off between cost and droop with the used high-impedance devices connected to it.

4.9.1.3 O1 (Impedance Converter)

The impedance converter, for our purpose, must

1. provide very high input resistance,
2. be single supplied,
3. offer rail-to-rail in- and outputs.
4. come with a low standby current

Op amps (OPA) are famously known for their almost ideal behaviour in terms of linear amplification, speed, accuracy, ease of use, low output impedance and high input impedance, but still most of the standard op amps do not fulfil requirements for our application as a large percentage of them need a dual voltage supply (e.g. $\pm 15V$), which our battery operated circuit cannot offer. And, although typically in the $G\Omega$ range already, an input resistance of this dimension would still cause a droop too large for our purpose. Op amps with larger input impedances are available, though. It is those ones who were made in a CMOS technology instead of a bipolar one, which come with an increased input impedance of three to four decimal powers.

Benchmark	**NJU7096M**	**NJU7091AF-TE1**	**MCP6032**	**MCP6052**
Supply Voltage [V]	1-5.5	1-5.5	1.35-5.5	1.8-6.0
Supply Current [μA]	200	15	1.35	30
Input Impedance [Ω]	1T	1T	1T	10T
Offset Voltage [μV]	?	?	$\pm$150	$\pm$150
Input Bias Current [pA]	1	1	1	1
Slew Rate [$\frac{V}{\mu s}$]	2.4	0.1	0.1	0.13
Gain-Bandwidth-Product	?	?	10	385
Output Type	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail
Number of Amplifiers	2	1	2	2
Price [USD]	0.64	0.34	0.34	0.34

Table 4.2: Comparison of different operational amplifiers for their suitability as impedance converter and voltage drop amplifier.

With a common mode input impedance of $10T\Omega$, a very high Open Loop Gain of $115dB$ and an output voltage swing range of $V_{SS}+15mV$ to $V_{DD}-15mV$, the Microchip MCP6052 fulfils our requirements (see comparison at table 4.2). It is a single supply op amp providing Rail-to-Rail In- and Outputs, low Offset Voltage of only $\pm 150\mu V$ although it has quite a low Gain Bandwidth Product of only $385kHz$ as well as a low slew rate of only $0.143\frac{V}{\mu s}$, which are both caused and compensated by the low quiescent current of only $30\mu A$. This remarkably low value makes it a highly recommendable candidate for long battery life time.

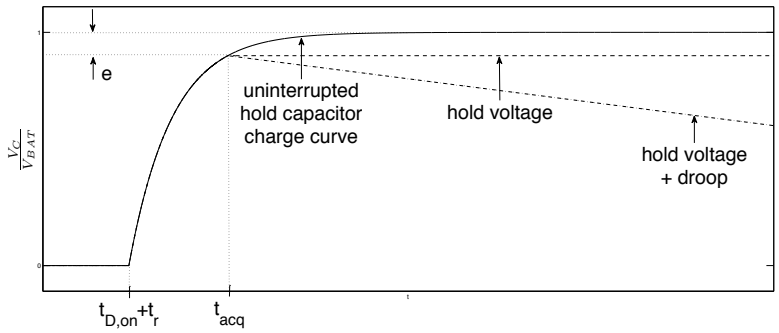


Figure 4.15: Sample and Hold signals.

Notable is the fact, that due to our limitation of a 3.3V power supply, this circuity is only operational for battery voltages of

$$V_{\text{BAT,min}} = 0.015V$$
$$V_{\text{BAT,max}} = 3.285V$$

as voltages below or above will be limited to these values. This covers the SOC Range 0-95% for $LiFePO_4$ batteries.

4.9.1.4 Calculation and Simulation

The given circuitry provided in figure 4.14 results in the time behaviour shown in figure 4.15.

The hold capacitor charging time constant using relay resistance R_{on} equals

$$\tau = R_{\text{on}}C = 0.1\Omega \cdot 100nF = 0.1ns, \tag{4.8}$$

which relates to a charging time t_{chrg} until the error e is below $1\mu V$ of

$$t_{\text{chrg}} = -\tau \cdot \ln(\frac{e}{V_{\text{BAT}}}) = 1.5ns. \tag{4.9}$$

In hold mode, the capacitor sees a total resistance of

$$R_{\text{hold}} = R_{\text{off}} \parallel R_{\text{O1,in}} = 5T\Omega \parallel 10T\Omega = 3.33T\Omega \tag{4.10}$$

which leads to an initial droop rate of

$$\frac{dV}{dt} = \frac{V_0}{RC} = \frac{3.2V}{3.33T\Omega \cdot 100nF} = 9.6\frac{\mu V}{s}. \tag{4.11}$$

The maximum charging current equals

$$I_0 = \frac{V_{\text{BAT,max}}}{R_{\text{DS,on}}} = \frac{4V}{0.1\Omega} = 40A, \tag{4.12}$$

effective for a very short time only and thus handleable by the relay.

4.9.2 Voltage Drop Amplifier

If a load is applied to the battery, the terminal voltage step response looks as shown in figure 4.16.

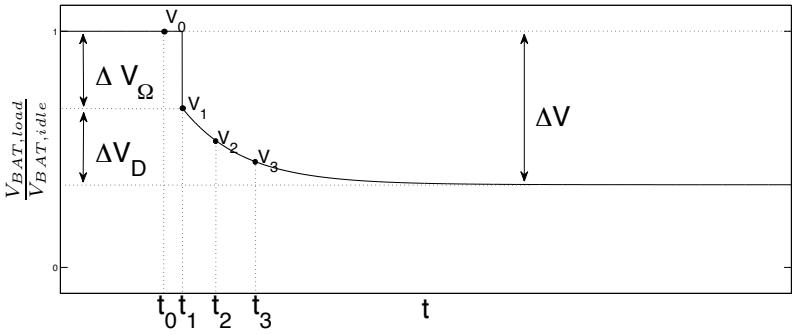


Figure 4.16: Battery terminal voltage step response after applying a load.

We want to take a look at the simplified EEEC as shown in figure 2.9b and see how the parameters can be obtained.

The terminal voltage $V_{\text{Term}}(t)$ after a current jump $I(t)$ at $t = t_1$ is given by

$$\begin{aligned} V_{\text{Term}}(t) &= V_{\text{BAT}} - \Delta V_\Omega - \Delta V_D \cdot \left(1 - \exp\left(-\frac{t}{\tau_D}\right)\right) \\ &= V_{\text{BAT}} - I(t)R_\Omega - I(t)R_D \cdot \left(1 - \exp\left(-\frac{t}{R_D C_D}\right)\right) \end{aligned} \tag{4.13}$$

with

$$I(t) = I_0 \cdot s(t - t_0) \tag{4.14}$$

$$s(t) = \begin{cases} 1, t \geq 0 \\ 0, t < 0 \end{cases} \tag{4.15}$$

The unknown parameters V_{BAT}, R_Ω, R_D and C_D can be derived by 4 measurements V_0, V_1, V_2 and V_3 at times t_0, t_1, t_2 and t_3, while $t_3 > t_2 > t_1 > t_0$.

V_0 must be measured before the current jump and V_1 *immediately* after. V_2 and V_3 can be sampled arbitrarily, but it is advisable to choose t_2 and t_3 such that a good trade-off between a small measuring time and a small ADC sampling error is achieved.

Condition	$\lvert\Delta V\rvert$
$\lvert I\rvert$ = 100mA, R_i = 20$m\Omega$ (1 cell)	2mV
$\lvert I\rvert$ = 100mA, R_i = 0.5$m\Omega$ (40 cells)	50μV
$\lvert I\rvert$ = 3A, R_i = 20$m\Omega$ (1 cell)	60mV
$\lvert I\rvert$ = 3A, R_i = 0.5$m\Omega$ (40 cells)	1.5mV

Table 4.3: Expectable voltage drop magnitudes for different conditions.

4.9.2.1 Voltage Drop Magnitude

A look at the expected voltage drops for different battery resistances and current jumps (see table 4.3) discloses that they need to be pre-amplified before being applied to the ADC. The ADC resolution of

$$1\text{LSB} = 244\mu V \tag{4.16}$$

would introduce a large quantizing error otherwise.

A reduction of the quantizing error can be achieved

1. by increasing the magnitude of the current jump $\lvert I(t)\rvert$ or
2. by an analogue pre-amplification of the voltage drop $\Delta V(t)$.

The problems with the first option are:

- Additional hardware is needed, at least another power resistor and transistor are needed, which are big and expensive.
- Higher magnitude of current jumps result in an increased dissipated power, which very quickly produces non-handleable thermal problems.
- Though short-term overshooting of the resistor's power rating is allowable, RC time constants at low SOC do not fall into this category.
- An increased energy dissipation of the battery for every measurement.
- PCB traces, as not being made for high currents, will introduce a significant voltage drop which leads to larger measurement errors.

Far better compared to the first approach is an analogue pre-amplification of the voltage drop, which shall be examined next.

4.9.2.2 Voltage Drop Amplifier

The voltage drop amplifier shall amplify the difference between the original battery voltage sampled by the hold capacitor and the dropping terminal voltage function, expressed in the following transfer function:

$$V_{\text{Out(t)}} = A \cdot \left(V_{\text{Sample}} - V_{\text{Term}}(t)\right) \tag{4.17}$$

The circuitry is shown in figure 4.17 As we are dealing with the same kind of op amp we

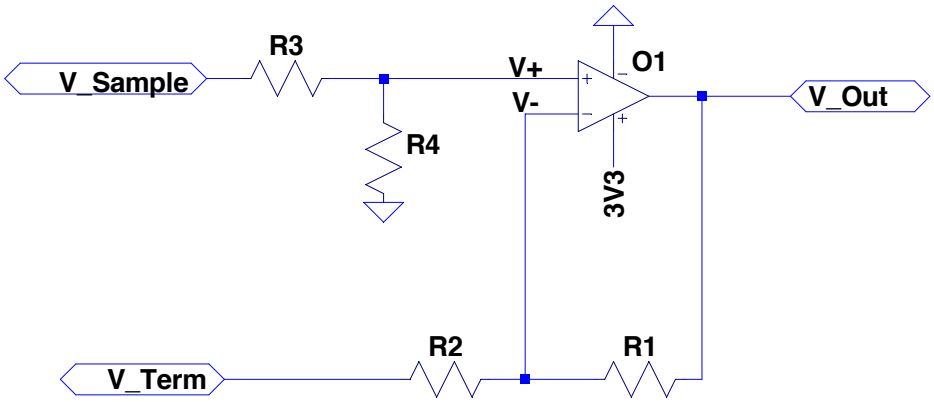


Figure 4.17: Voltage drop amplifier. The single-ended operational amplifier is used as a differential amplifier.

also use for the sample and hold impedance converter, which is not a differential but a single ended amplifier, we are using a little trick to make it work like a differential amplifier. With the given circuitry, the output voltage can be calculated as follows:

$$\begin{aligned} V_{\text{Out}} &= \frac{(R_1 + R_2)R_4}{(R_4 + R_3)R_1} V_{\text{Sample}} - \frac{R_1}{R_2} V_{\text{Term}} \\ &= \left(\frac{R_2 + R_1}{R_2}\right)\left(\frac{R_4}{R_4 + R_3}\right) V_{\text{Sample}} - \frac{R_1}{R_2} V_{\text{Term}} \end{aligned} \tag{4.18}$$

The differential input impedance is approximately

$$Z_{\text{IN}} = R_2 + R_3 \tag{4.19}$$

By choosing

$$R_1 = R_4 \tag{4.20}$$

$$R_2 = R_3 \tag{4.21}$$

$$\tag{4.22}$$

the voltage difference $V_+ - V_-$ is zero for $V_{\text{Sample}} = V_{\text{Term}}$ and thus $V_{\text{Out}} = 0$. The output voltage expression simplifies to

$$V_{\text{Out}} = A(V_{\text{Sample}} - V_{\text{Term}}) \tag{4.23}$$

with the amplification factor

$$A = \frac{R_1}{R_2} \tag{4.24}$$

which represents the desired behaviour.

The amplification factor must be chosen accordingly to the maximum expectable block impedance.

Figure 4.18 shows a simulation of a $2mV$ voltage drop which is amplified to $1V$ (the ADC reference voltage) using an amplification factor of $A = 500 = 54dB$ showing the expected result. This voltage drop would result from a current jump magnitude of $|\Delta I| = 100mA$ at an inner resistance of $R_i = 20m\Omega$. Care must be taken when choosing amplification factors closer to the open loop gain as the formula 4.23 becomes inaccurate. It is not advisable to go beyond amplification factors of $A = 1000 = 60dB$ and use the built-in ADC pre-amplifier, if additional amplification is needed.

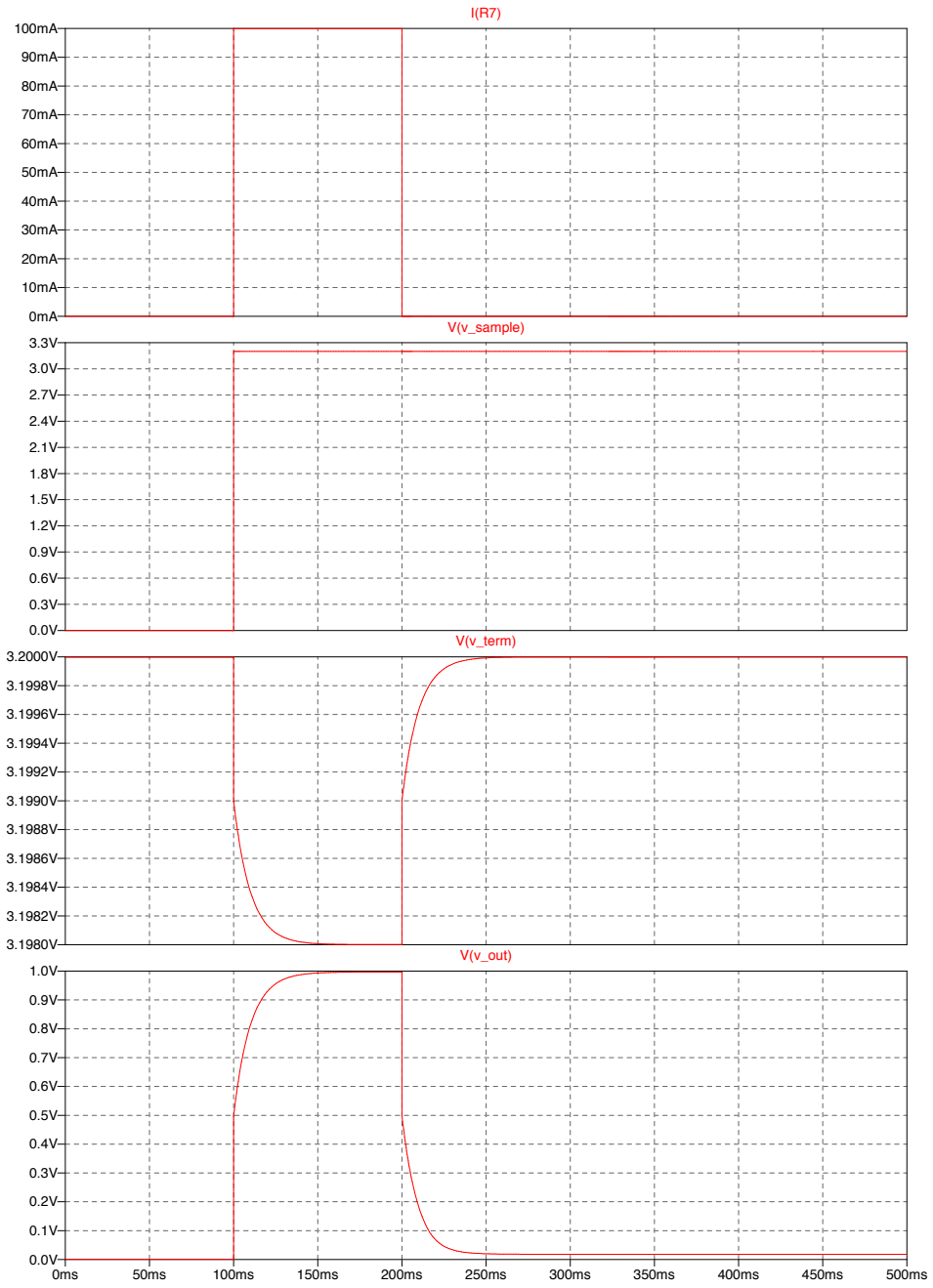


Figure 4.18: Voltage drop amplifier simulation using $R_i = 20m\Omega$, $C_D = 1F$ and $A = 500$.

4.10 Balancing

Balancing is needed for equalizing charge in each battery block to maximize the total amount of storable energy in the battery pack. We discussed several active and passive balancing techniques in chapter 3.3 and want to make use of that knowledge to use the best possible technique for our experimental platform.

The main constraint which prevents us from using a non-energy-wasting active balancing approach is the ease-of-installation requirement. All active balancing solutions require wiring across battery blocks to transfer energy. As our platform stands out by not using any interconnects, using additional wiring for balancing would conduct the effort ad absurd um.

This leaves us with passive balancing, which should occur at the top of SOC, as discussed in chapter 3.3.

- Charge the pack while monitoring all block voltages. Once one block leaves the flat plateau, start bypassing charging current across the cell and gradually increase it as the SOC comes closer to 100% SOC. This approach requires relatively large bypass currents, as it must work within a short period of time, but works also without precise knowledge of the SOC. This option will be discussed in section 4.10.1.
- Precisely monitor SOC and balance all the time, no matter whether charging, discharging or idle. This method can work well with low currents, as it's having plenty of time to do the work. We discuss this option in detail in section 4.10.2.

4.10.1 P-Balancing

P-Balancing refers to the principle of a P-Controller in control systems: An actuating variable is adjusted by measuring the error of a control variable and multiplying it by a constant factor. It can be realized by a circuitry given in figure 4.19. A desired value can be generated by the DAC provided from the Microcontroller. Alternatively, a pulse-width-modulated signal with an optional low pass filter can be used. The op amp O1 adjusts the gate voltage V_G such that

$$V_{DAC} - V_{fb} = 0 \tag{4.25}$$

by adjusting the n-channel MOSFET resistance R_{DS} accordingly. The balancing current I_{BAL} creates a voltage drop across the small-valued current sensing shunt resistor R_{SH}, V_{SH}, which is amplified through O2 to the value of

$$\begin{aligned} V_{fb} &= \left(1 + \frac{R_1}{R_2}\right) V_{SH} \\ &= \left(1 + \frac{R_1}{R_2}\right) I_{BAL} R_{SH}. \end{aligned} \tag{4.26}$$

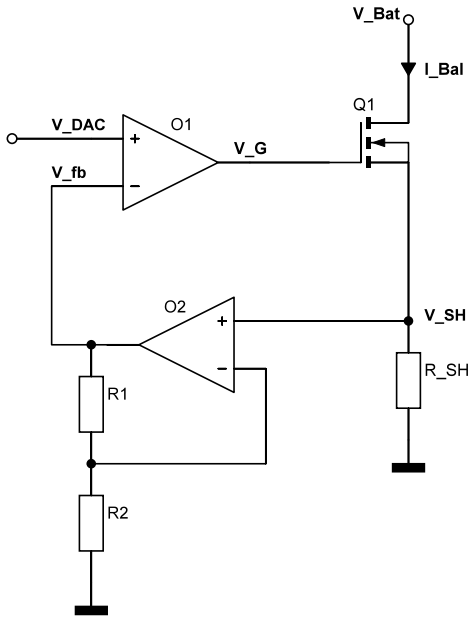


Figure 4.19: P-Balancing. The balancing current I_{BAL} can be adjusted linearly by an arbitrary voltage created by the DAC.

The balancing current is

$$I_{BAL} = \frac{V_{DAC}}{A \cdot R_{SH}} \tag{4.27}$$

with

$$A = 1 + \frac{R_1}{R_2}. \tag{4.28}$$

As $R_{DS} \gg R_{SH}$, the bulk power is dissipated by the MOSFET. The maximum balancing current is limited by the maximum dissipatable transistor heat P_{MAX} and given by

$$I_{BAL,max} = \frac{P_{MAX}}{V_{BAT}}. \tag{4.29}$$

It can be easily be scaled to the wanted maximum balancing time. What makes this circuitry attractive is it's simplicity, scalability and linear adjustability. The non-linearity of the transistor is compensated by the feedback signal derived from V_{SH}.

Application as Heater

This circuitry could also be used as a *heating application*. If the cell temperature drops below it's safe temperature range, the balancing circuit could be used as an adjustable heater to prevent damage to the cell.

4.10.2 Bang-Bang-Balancing

Bang-Bang-Balancing refers to the character of controlling the balancing current: on and off. It can be realised with either bipolar or MOSFET transistors as switches and a resistor to dissipate the heat. Bipolar circuits, as being current controlled, require an additional base resistor and should make use of low V_{CE} saturation voltage type transistors such as Philipp's PBSS4230T to make them not dissipate much heat and to make the balancing current mostly dependant on the choice of the balancing resistor R_{BAL} only.

The maximum allowable value of the base resistor can be calculated as

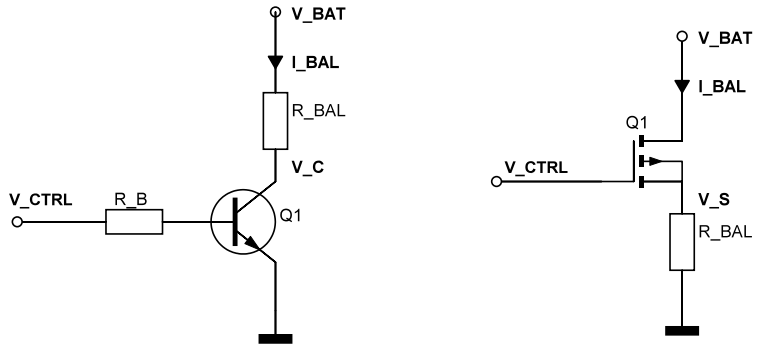
$$R_{B,max} = \frac{V_{SUP} - V_{BE,sat,max}}{I_{BAL}} \cdot h_{FE,min} \tag{4.30}$$

using the supply voltage V_{SUP}, the maximum saturation voltage $V_{BE,sat,max}$, the balancing current I_{BAL} and the minimum current amplification factor $h_{FE,min}$. Choosing a value $R_B < R_{B,max}$ allows for a higher balancing current I_{BAL}.

The maximum balancing current depends on the maximum power dissipation of the balancing resistor and is given by

$$I_{BAL,max} = \frac{P_{MAX}}{V_{BAT} - V_{CE,sat}}. \tag{4.31}$$

The use of MOSFETs is not recommended as the limited supply voltage at the gate of $V_{GS} = 3.3V$ is not sufficient to saturate the transistor for higher drain currents than a few hundred Milliamperes. If not saturated, the transistor works in a linear operation mode which incurs a large voltage drop across the drain and source, which affects the adjustability of the balancing current by the appropriate resistor value. A circuitry for both types of transistor is given in figure 4.20.



(a) (b)

Figure 4.20: Bang-Bang-Balancing Circuits (a) using bipolar transistor (b) using PMOS transistor.

5 Verification

5.1 Communication

The developed PLC functionality is tested in order to answer questions concerning reliability and constraints. For all tests, a PC transmits test messages via RS232 to Slave 1 which forwards the test message to Slave 2 over the power line. Slave 2 decodes the distorted message and sends it back to the PC, which categorizes the received byte as

- "OK", if the sent message equals the received message,
- "Error", if the sent message does not equal the received message,
- "Noise", if a message was received without a prior transmission or
- "Miss", if no message was received after a transmission.

Additionally, so called re-sync events are registered. Re-syncs take place after three erroneous received bytes. Figure 5.1 shows the channel model.

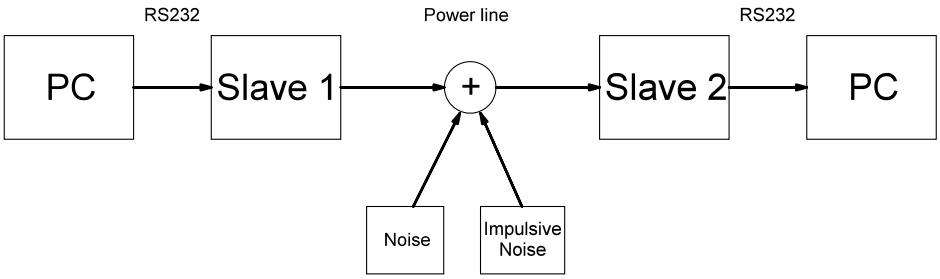


Figure 5.1: Channel model used for communication tests.

A PC transmits test signals, which are first converted to CMOS levels by a *MAX232* level converter to shift from RS232 ($\pm 15V$) to CMOS levels (3.3V/0V) and vice versa. Then, they are forwarded to the Master. The Master or slave 1 forwards it to the powerline where it reaches the slave or slave 2. The Slave decodes the message and sends it back to the PC using it's UART. That is only possible because all devices share a common ground.

The RS232 interface is configured in 1s8b1s mode, that means one message consists of one start bit, eight data bits and is terminated by a stop bit at a baud rate of

$$f_b = 19.200 \frac{baud}{s} \tag{5.1}$$

which equals a data rate of

$$f_d = 1.92\frac{\text{kB}}{\text{s}}. \tag{5.2}$$

For the PLC transmission, a carrier frequency of

$$f_c = 5.5MHz \tag{5.3}$$

is used.

Signal bursts run for approximately 60 seconds or 115.200 bytes.

First of all, a basic verification using a DC power supply, is conducted. Compared to large batteries, it stands out by a comparably large inner resistance and an adjustable voltage, thus offering mild conditions for a first test.

5.1.1 Communication over Power Supply

Two BMS slaves are connected in parallel to a 0-30V 0-2.5A low dropout (LDO) voltage regulating DC power supply (Manson EP-613) (see 5.2). The voltage is adjusted from 1V-5.5V to reveal

- the minimum voltage for operation,
- the influence of the slaves' DC/DC converters when operated in step-down (LDO) mode (input voltages > 3.3V) and
- the communication behavior when the DC/DC converter is in step-up (switching) mode (input voltages $\leq$ 3.3V).

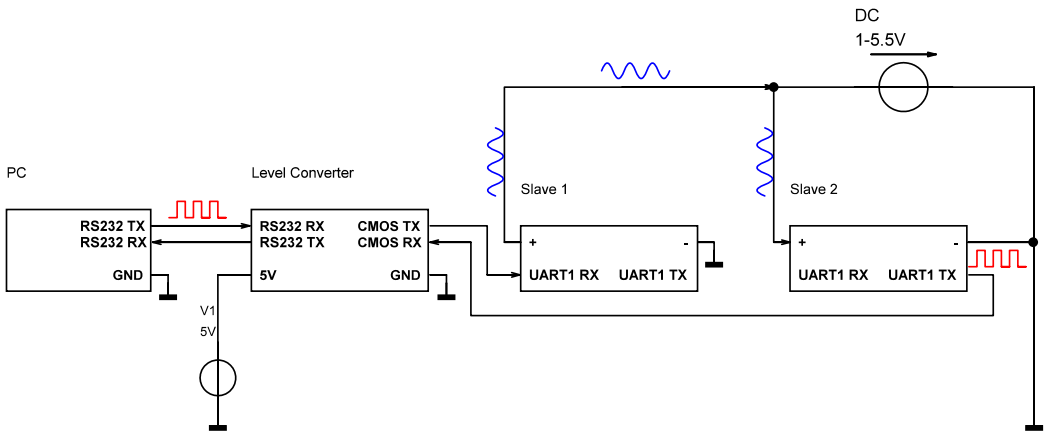


Figure 5.2: Communication over Power Supply test setup. Both devices are connected in parallel.

The communication works perfectly for the full voltage range of 2.0V-4.0V, as shown in figure 5.3. Beyond that, communication down to 1.5V is still 100% reliable. That is the case when the DC/DC converter stops working.

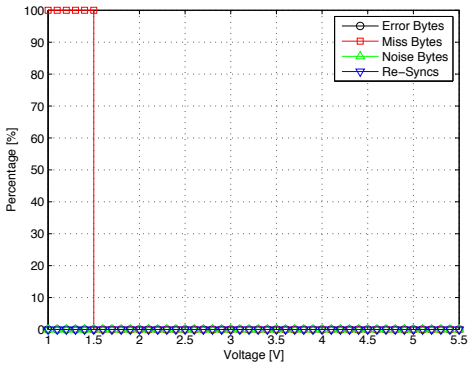


Figure 5.3: Byte error ratio for two slaves connected in parallel to the same DC power supply of variable voltage. An error rate of 0.00% is measured for voltages above 1.5V.

5.1.2 Communication over Battery Block

The power supply is now replaced by a Thundersky 3.2V $LiFePO_4$ 90 Ah (WB-LYP90AHA) battery as shown in figure 5.4. Although it has an inner resistance of less than $1m\Omega$ which is a lot lower than the DC power supply, RX signal levels almost stay the same and so do the bit error rates: 0.00% errors occur in this test as well, as the results in figure 5.5 show. Apparently, the series inductance of the battery (see figure 2.9c), typically in the range of a few hundred Microhenrys at that capacity, prevents the high-frequency TX signal from being attenuated by the battery.

5.1.3 Communication over Battery Pack

Since a battery management system needs to report data of each cell over a chain of cells, the next interesting question arising is: how well does this kind of communication work. As shown in figure 5.6, this setup uses two 3.2V $LiFePO_4$ batteries to create a minimalistic battery pack. One slave board acts as master module (connected to the pack voltage of 6.4V) while the other one acts as slave (connected to a single block of 3.2V). Common ground for RS232 transmission is the negative pole of battery 2.

Figure 5.7 shows a spectrogram of the RX signal after having passed the decoupling capacitor C4 of figure 4.4. It shows distinctive peaks at the carrier frequency of 5.5MHz and it's harmonics at 11MHz, 16.5MHz and so forth. The fundamental peak at 5.5MHz is approximately 42dB from the noise floor which is a value that would allow a lot faster communication speeds than 19.200bps with the Shannon limit indicating a channel capacity C

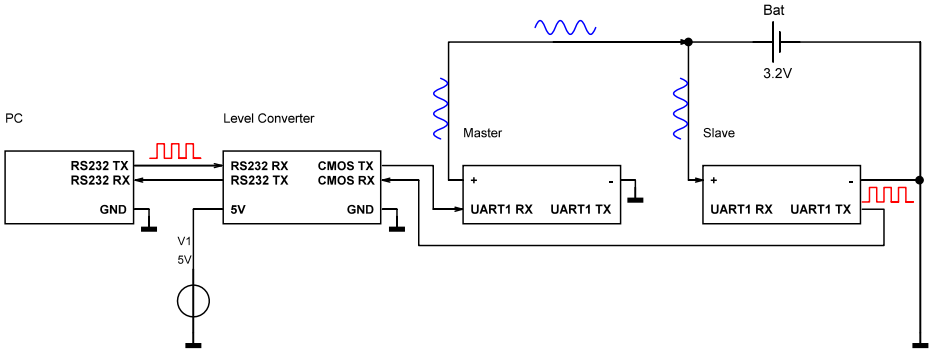


Figure 5.4: Communication over Battery Block setup. Both devices are connected in parallel.

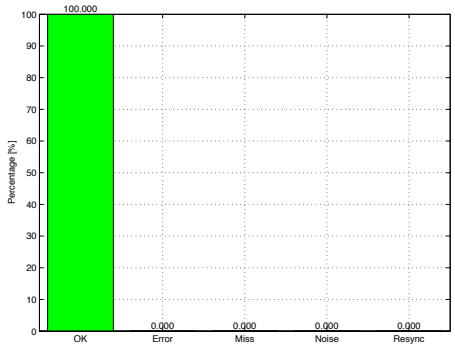


Figure 5.5: Communication over a Battery Block works without any errors.

of 8.87MBit/s for that channel according to Shannon's law

$$C = B \cdot \log_2 \left(1 + \frac{S}{N}\right) \tag{5.4}$$

with signal energy S, noise energy N and bandwidth B. The signal-to-noise ratio can often be estimated by checking the spectrum analyzer: As long as the resolution bandwidth R is bigger than the signal bandwidth B or equals it, the S/N ratio can be read from the spectrogram as the distance to the noise floor.

Another observation from the spectrogram is a high total harmonic distortion (THD) which is defined as the ratio of the energy of all harmonics H_i and the energy of the fundamental wave F. This behaviour is not tolerable in shared mediums but does not

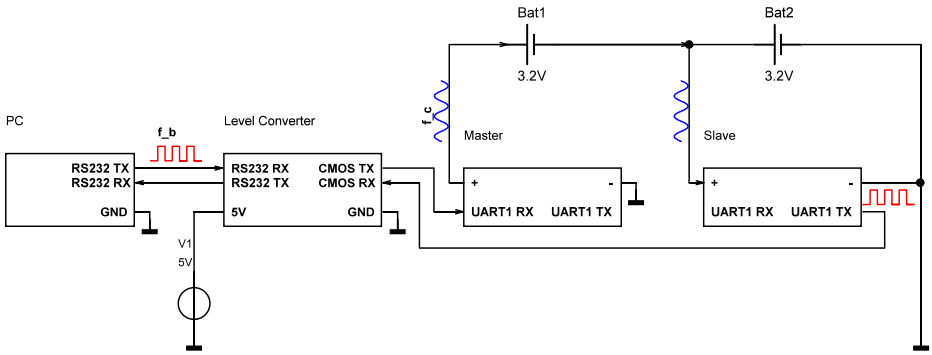


Figure 5.6: One-way Master-Slave-Communication setup using a minimalistic battery pack consisting of two batteries in series. A PC is used to send test data to the Master, which forwards the data to the Slave using the power line. The Slave decodes data and sends it back to the PC using it's UART. The PC compares sent data with received data and classifies the received data bytes as "OK", "Error" or "Noise" and also counts "Miss" bytes and Re-Sync Events.

cause any harm in this case.

$$THD = \frac{\sqrt{\sum_{i=1}^{N} H_i^2}}{F} \tag{5.5}$$

Figure 5.7: Spectrum of the RX signal from 0 to 50MHz. Remarkable are the carrier frequency of 5.5MHz and it's harmonics, which are not filtered very well, causing a large total harmonic distortion which could interfere with other devices on the power line and even radiate into the air, especially when the power line is long.

Figure 5.8 shows the PLC spectrum centered around the carrier frequency $f_c = 5.5MHz$. The bandwidth is $B = 636kHz$.

The decoded results are faultless, however, and can be seen in figure 5.9. At reasonable Signal-To-Noise-Ratios (S/N), communication works without any errors.

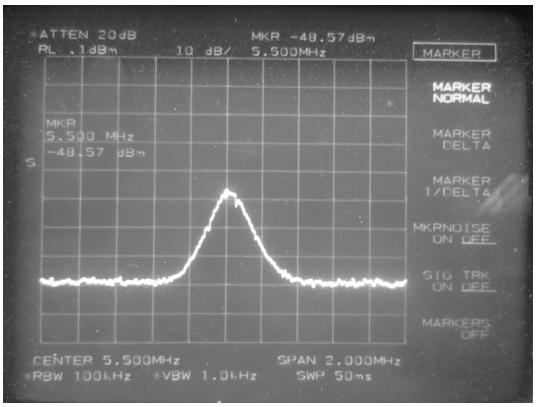


Figure 5.8: PLC spectrum around carrier frequency.

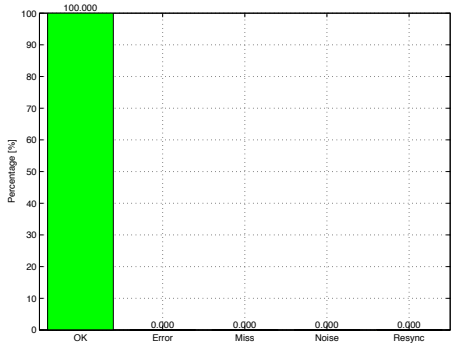
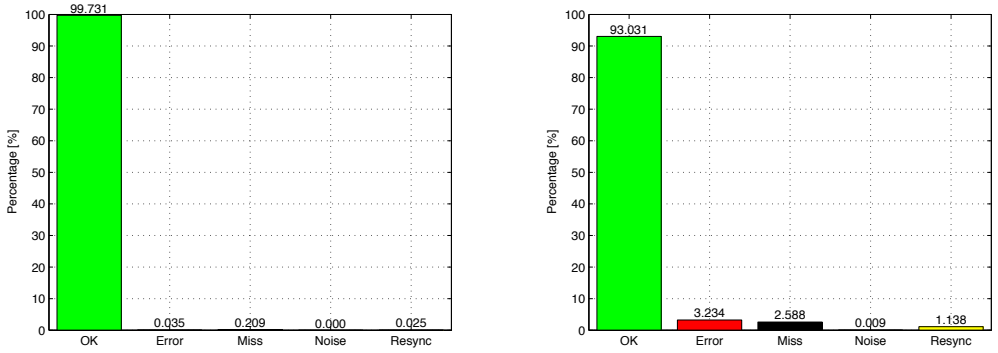


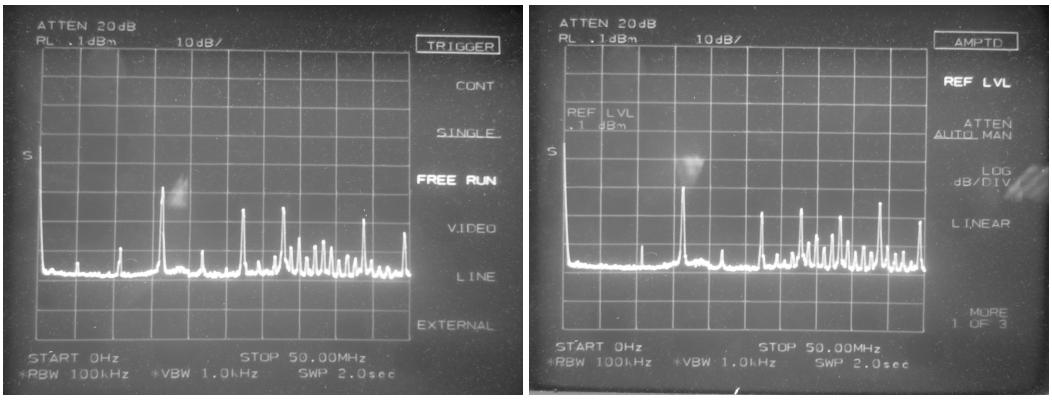
Figure 5.9: One-way Master-Slave-Communication over a battery pack works perfectly.

5.1.4 Communication over Battery Pack with Attenuation

An interesting question arising after having seen the battery pack communication setup working perfectly at high S/N levels is the question, at which S/N level the PLC IC starts producing errors. For this purpose, a cutoff-frequency variable low pass filter is used in series with the battery blocks to attenuate the signal. The results which are partially shown in figure 5.10 have demonstrated that $S/N = 5dB$ is the critical level at which the first transmission errors occur. Data tend to get lost first ("Miss Bytes") as the S/N decreases and are then decoded wrongly. This is surprising, since it would be expected to be the other way around. Once one byte has been decoded falsely, there is a high chance that the next two bytes are, as well, causing a re-sync event in consequence.



(a) (b)



(c) (d)

Figure 5.10: Results of the communication over battery pack with attenuation tests. (a) and (c) S/N = 3dB, (b) and (d) S/N = 0dB.

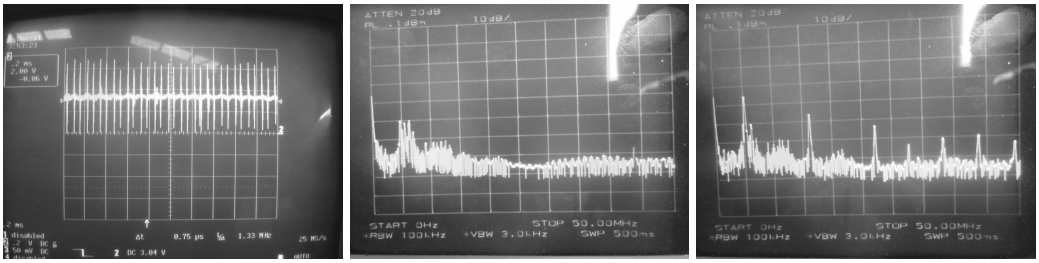
5.1.5 Communication in an Electric Vehicle

Finally, a communication test within the battery pack of an operational real-world electric vehicle is carried out. An electric Ford Focus (shown in image 5.11) was used for these purposes. Insight into technical data can be gained from table 5.1.5.

(a) (b)

Figure 5.11: An electric Ford Focus is used for electric vehicle communication tests.

Electric vehicle power lines are piled with impulsive noise due to switching of large currents of the DC power line (figure 5.12a), mainly caused by the motor controllers to control the revs, but also by other devices like the DC/DC converter which powers the standard 12V devices.



(a) (b) (c)

Figure 5.12: Oscilloscope and spectrum analyzer snapshots under heavy load. (a) Switching voltage spikes on the oscilloscope. (b) Frequency spectrum 0-50MHz without transmission. (c) Frequency spectrum 0-50MHz with transmission. The increased noise level around 5.5MHz (b) causes a lot of wrongly decoded "noise bytes" when no transmission occurs. However, their appearance probability is drastically decreased when a transmission, which emerges clearly from the noise spectrum, takes place.

As it is an asset to a car to have a high range, big battery packs are used. Big battery packs come along with low inner impedances and do not necessarily offer good conditions

Base Car	
Base Vehicle	2011 Ford Focus Sedan, manual, 5-seater
Drivetrain	5sp manual, front wheel drive
Curb Weight	same as combustion model
Electrical Parts	
Motor	Netgain Impulse 9
Motor Controller	EVnetics Soliton1
Battery Pack	45x ThunderSky LFP160AHA ($LiFePO_4$, 3.2V, 160Ah)
Pack Voltage	144V
Capacity	23kWh
Maximum Current	480A
Maximum Power	80kW
DC/DC Converter	Iota DLS-55
Brake Assist	Electric vacuum pump
Power Steering	Electric power steering pump
Heater	Electric heater
Air-conditioner	Belt driven
Battery Management	EV Power
Performance	
Top Speed	130km/h
Range	130km
Charger	Protech TCCH-45C-08A 144V single/three-phase
Charging Time	10h (single-phase), 3h (three-phase)

Table 5.1: Technical data of the Ford Focus electric test vehicle, as provided on `http://www.therevproject.com`.

for communication. For example, where it is common practice in communication engineering to match the source resistances with the wave resistance of the cable to maximize the transmitted power into the cable and to avoid reflections resulting in standing waves and Rayleigh-Fading, it is not possible to match impedances using a powerline, as the wave impedance depends on the geometry of the cabling. For these reasons, an electric vehicle is the ultimate worst-case scenario and thus, it is most suitable to answer the question whether or not power line communication is a viable solution for battery management systems.

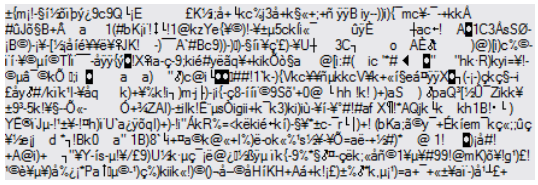


Figure 5.13: Wrongly decoded noise bytes, while car under load and no transmission taking place.

Like before, the battery pack of the test vehicle is fitted with two BMS modules, one connected to a single 3.2V block and acting as a slave and the other one connected to two single blocks, sharing a common ground with the laptop for RS232 communication (see figure 5.14).

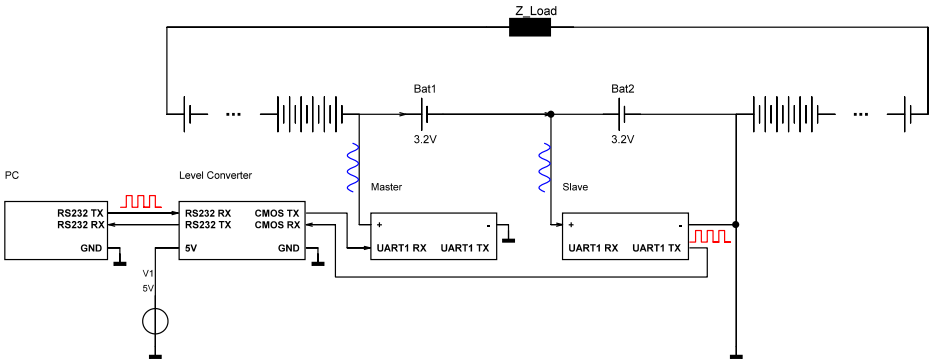


Figure 5.14: Communication in an Electric Vehicle test setup. Communication capability over a large battery pack consisting of 45 $LiFePO_4$ batteries of 160Ah blocks shall be examined for different load scenarios. Complex impedance Z_{LOAD} is representative of all load connected to the HV battery pack, i.e. the motor controllers and DC/DC converter *et cetera*

The laptop is running on battery mode to not create an earth loop capable of capturing additional noise. Oscilloscope snapshots and frequency spectra are taken and communication reliability is measured under different load scenarios:

- Car off (integrity check - should provide similar results compared to the "communication over battery pack" results).

- Ignition and all electrical devices on
- Revving with almost no load on the engine
- Revving with load on the engine

During the tests, the most variable benchmark was the rate of captured noise bytes, as shown in figure 5.15.

While the engine is turned off, no noise bytes are captured and communication works reliably. On ignition and with no transmission, a few noise bytes are captured due to the increased noise floor introduced by the DC/DC converter. The occurence of noise bytes increases drastically when the motor controllers powers the engines. However, they almost completely disappear when a concurrent transmission takes place.

Figure 5.16 shows the final result for the communication in an electric vehicle under load transmission test. With a correct transmission rate of 99.937%, it can be concluded that communication works very reliably even under worst conditions.

5.1.6 Conclusions

To conclude this section, it can be stated that:

- Powerline communication works reliably, even in the worst-case scenario of an electric vehicle under load.
- An increased number of noise bytes while no transmission takes place needs precautions in terms of simple channel coding.
- Significant line attenuation due to the length of the power line could not be observed.
- Parallel capacitances to the individual power supply can massively attenuate the HF signal and such a HF short-circuiting must be prevented.
- From a communications engineering point of view, it can be stated that the transmission works reliably down to S/N levels of 5dB of the main carrier frequency.
- A lot of the available channel capacity is still unused and further research towards an integration of larger parts of electric car communication into the powerline can be conducted. A common usage of the high voltage power line and the low voltage power line is possible.

Because of these aspects, Powerline Communication can be called a viable solution to replace communication wires.

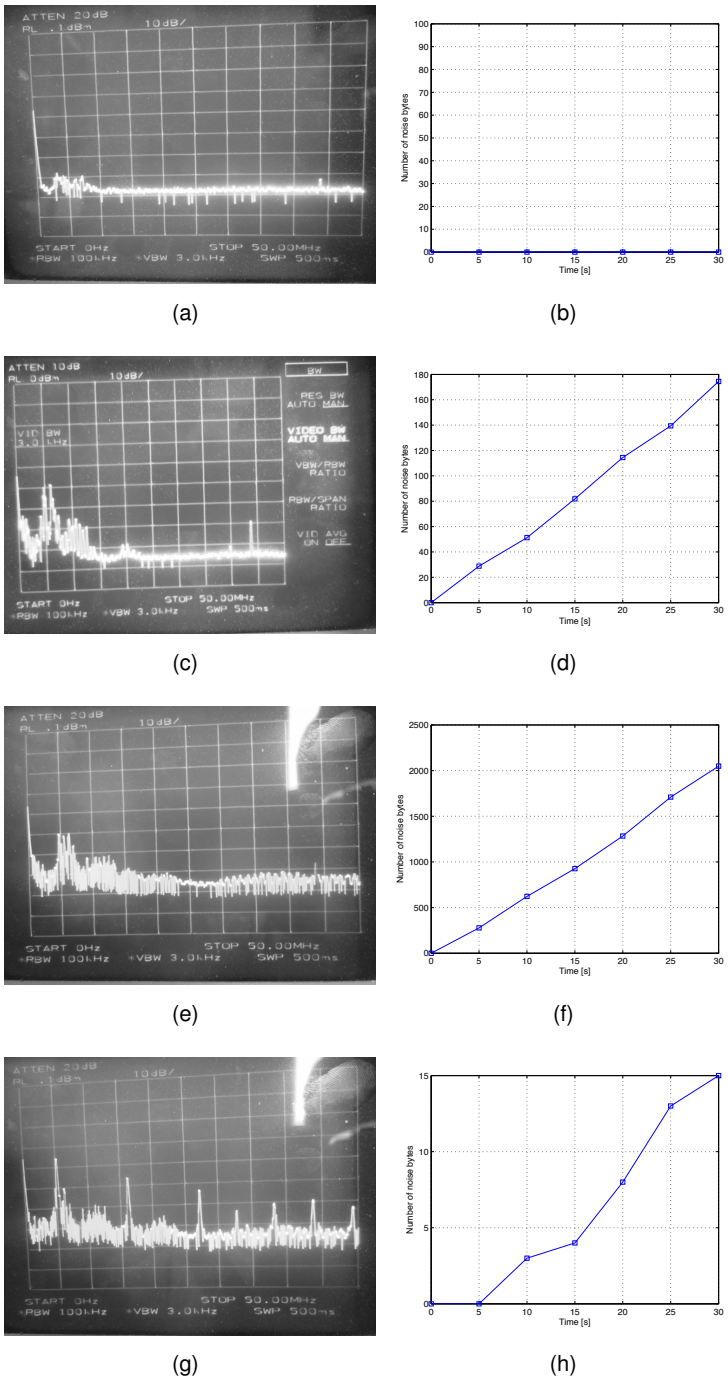


Figure 5.15: Communication in an Electric Vehicle test results (1). Spectrograms and number of noise bytes captured for scenarios (a,b) Off, no transmission (c,d) Ignition, no transmission (e,f) Engine revving with 30kW load, no transmission (g,h) Engine revving with 30kW load, with transmission.

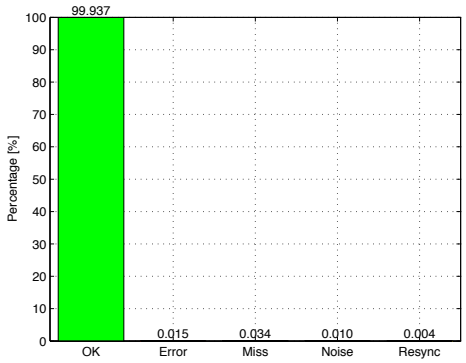


Figure 5.16: Communication in an Electric Vehicle test results (2): under load, with transmission taking place.

5.2 Inner Parameters

Using the voltage drops shown in figure 5.18, the inner parameters of a K2 LFP26650EV $LiFePO_4$ 3.2Ah battery shall be determined. The model to be parametrized is the simple EECE, as shown in figure 5.17, consisting of

- an ohmic resistance R_Ω,
- the fast-acting diffusion overpotential resistance R_D and capacitance C_D as well as the time constant $\tau_{R_D C_D}$,
- the slow-acting concentration overpotential resistance R_C and capacitance C_C and the according time constant $\tau_{R_C C_C}$ and
- the open circuit voltage V_{BAT}.

These parameters are determined over the full range of states of charge, as $R_\Omega = f(\mathrm{SoC})$ and $\{R_D, C_D, R_C, C_C, V_{\mathrm{BAT}}\} = f(\mathrm{SoC,t})$.

Answers to the following questions are sought:

- What is the range of values to expect, and what variances are to expect?
- Which values are suitable best to deduct the state of charge?
- What influence does the current jump magnitude have on the measurements?
- Which edge, the falling one or the rising one, provides more accurate results?
- What minimum voltage drop magnitude is needed for an unamplified measurement, and can the limit be pushed using the previously designed analog voltage drop amplifier?

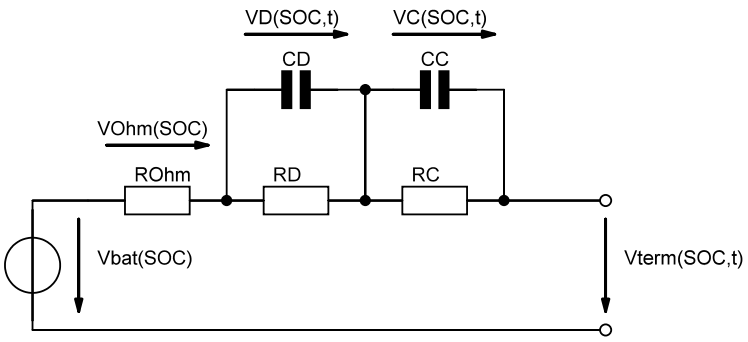


Figure 5.17: Electrochemical Electrical Equivalent Circuit with the parameters R_Ω, R_D, C_D, R_C, C_C and V_{BAT} to be determined for different states of charges.

Finally, the obtained parameters are used to calculate the complex impedance which is illustrated in a Nyquist Plot.

Figure 5.18 shows the voltage drop and recovery procedure in detail, which is the base for all three subsequent experiments, which are conducted at different discharge rates.

5.2.1 High Discharge Rate Unamplified Measurement

5.2.1.1 Setup

We start off the experiment by choosing a large initial discharge current of $i_{\text{dis}} = 2.26A/7.2W$ or $0.7C$, which is derived from the applied discharge resistor of $R_{\text{dis}} = 1.3\Omega$, with a setup as illustrated in figure 5.19. We further use a period setting of $T_{\text{dis}} = 60s$ and $T_{\text{rec}} = 30s$ to obtain a reasonably fine-gridded SoC resolution and a large recovery time to give the battery a chance to settle at the true open circuit voltage including all overpotentials before further discharge continues.

5.2.1.2 Capacity

Before doing the actual parameter estimation, the ability of the Battery Management System to determine the capacity of a battery shall be proven. Therefore, a K2 LFP26650EV 3.2V / 3.2Ah $LiFePO_4$ battery is discharged over a $R_{\text{Dis}} = 1.3\Omega$ resistance at an (initial) 0.7C rate while monitoring the terminal voltage. Figure 5.20 shows the results. While the cell shows the characteristic voltage curve of a $LiFePO_4$ battery with a flat plateau for DoDs

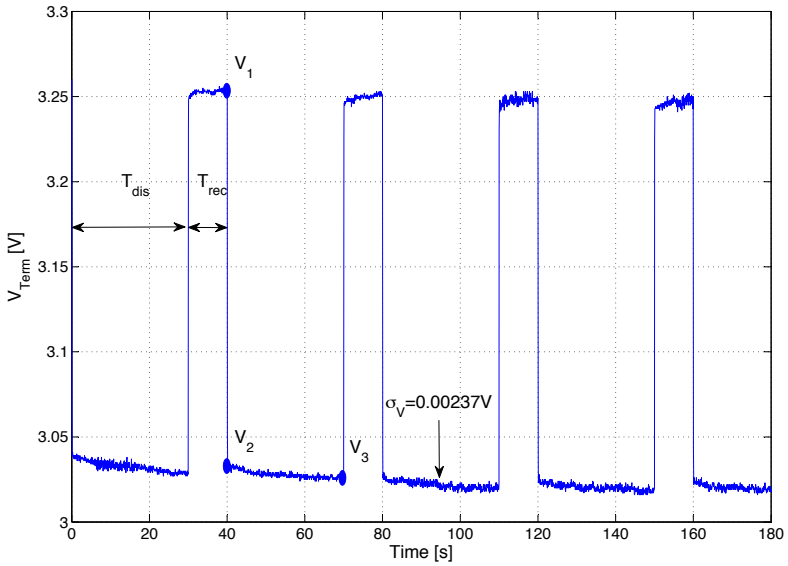


Figure 5.18: Voltage drop procedure in detail. Discharge periods of duration T_{dis} are followed by recovery periods of T_{rec}. Voltage V_1 is the last sample before a current jump, rising or falling, V_2 is the sample right after and V_3 the last sample before the opposite edge. All recorded samples, sampled at a rate of f_s, are subject to measurement noise introduced by the ADC with a standard deviation of σ_V.

of up to 80% and an exponentially decreasing voltage afterwards, the nominal capacity of 3.2Ah has already fallen to less than 2Ah in this example. The slope of the energy degree of discharge decreases over time as the terminal voltage decrease. The balancing current is obtained by calculating

$$I_{\text{BAL,i}} = \frac{V_{\text{Term,i}} - V_{C,i}}{R_{\text{BAL}}}. \tag{5.6}$$

This is used for calculating the depth of discharge as

$$\text{DoD(t)} = \sum_{i=1}^{f_s t} I_{\text{BAL,i}} \tag{5.7}$$

and the energy depth of discharge as

$$\text{DoD}_{\text{E}}\text{(t)} = \sum_{i=1}^{f_s t} V_{\text{Term,i}} \cdot I_{\text{BAL,i}}, \tag{5.8}$$

respectively.

Next, we have a look at the inner parameters, starting with the diffusion overpotential and ohmic parameters.

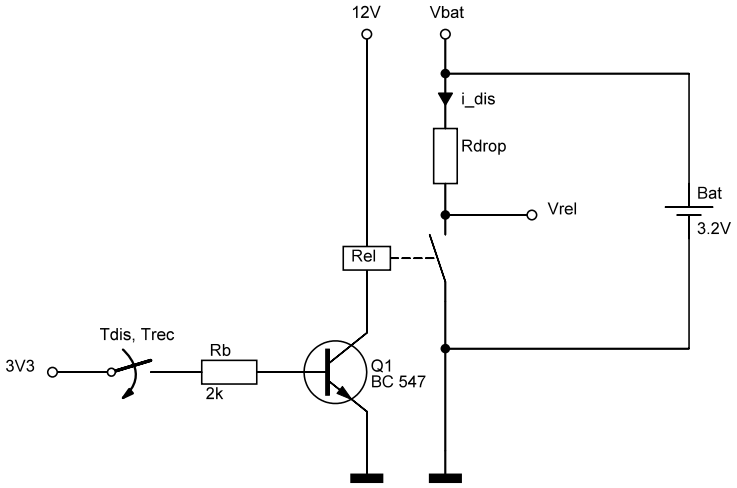


Figure 5.19: High discharge rate voltage drop setup. The battery is discharged over R_{Drop} with the discharge current i_{dis} for a period of t_{dis}, followed by a recovery phase of t_{rec} and then repeated. During all the time, the battery voltage V_{BAT} is captured and later used to calculate the inner parameters of the battery. The potential V_{Rel} is used to calculate i_{dis} and track the degree of discharge. An external 12V relay, triggered by the slave, is used to enable high discharge currents and, maybe even more important, to seperate large discharge currents from the PCB, which would otherwise create a significant voltage drop across the thin PCB routes and the ground plane, significantly enlarging and distorting the measured inner impedance. The use of the relay comes at the price of a relatively large settling time of approximately 1.5ms, making the automatized measurement of the diffusion overpotential parameters difficult.

5.2.1.3 Diffusion Overpotential and Ohmic Parameters

Diffusion is a process with a relatively low time constant of several milliseconds. Therefore, we increase the sampling rate to $f_s = 1000Hz$ and sample 185 values. These values are trade-offs between the limited memory resources in the microprocessor, a resolution fine enough to capture the details in the beginning and coarse enough to see the final settling voltage. Limited computational resources in the microprocessor do not leave a lot of room for averaging, resulting in noisier data. Figure 5.22 shows the transients at different degrees of discharge and figure 5.21 shows the calculated values of R_D, C_D and the associated time constants τ_{RC}.

The EEC parameters are calculated by taking three samples $V_1(t_1)$, $V_2(t_2)$ and $V_3(t_3)$ according to figure 5.18. They are used to calculate a first approach to the inner parameters by explicitely solving equation 4.13 for the parameters

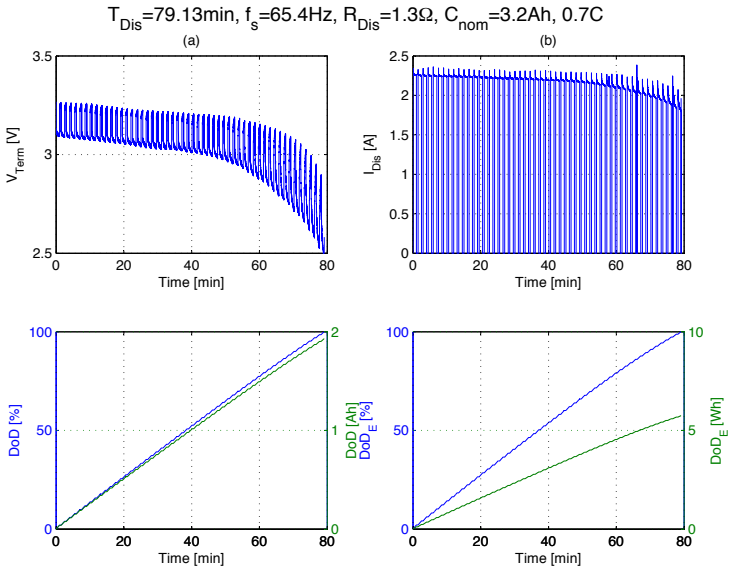


Figure 5.20: Capacity Determination of a $LiFePO_4$ battery of nominal capacity of $C_{\text{nom}} = 3.2Ah$.

$$R_\Omega = \frac{V_1 - V_2}{I_{\text{BAL}}}, \tag{5.9}$$

$$R_D = \frac{V_2 - V_3}{I_{\text{BAL}}}, \tag{5.10}$$

$$C_D = \frac{1}{\ln\left(1 + \frac{V_3 - V_1 + I_{\text{BAL}} R_\Omega}{I_{\text{BAL}} R_D}\right) \cdot \left(-\frac{R_D}{t_3}\right)}. \tag{5.11}$$

These start values are used to iteratively calculate a best fit of the equation

$$V_{\text{term}}(t) = V_1 + i_{\text{dis}} \cdot R_D \cdot \left(1 - \exp\left(\frac{-t}{R_D C_D}\right)\right) = F \tag{5.12}$$

by finding coefficients

$$\vec{\mathbf{x}} = \begin{bmatrix} R_D \\ C_D \end{bmatrix} \tag{5.13}$$

that solve the problem

$$\min_x \| F\left(\vec{\mathbf{x}}, \vec{\mathbf{x}}_m\right) - \vec{\mathbf{y}}_m \|_2^2 \tag{5.14}$$

$$= \min_x \sum_i \left(F\left(\vec{\mathbf{x}}, \mathrm{x}_{m,i}\right) - \mathrm{y}_{m,i}\right)^2 \tag{5.15}$$

given measured input data $\vec{\mathbf{x}}_m$ and $\vec{\mathbf{y}}_m$.

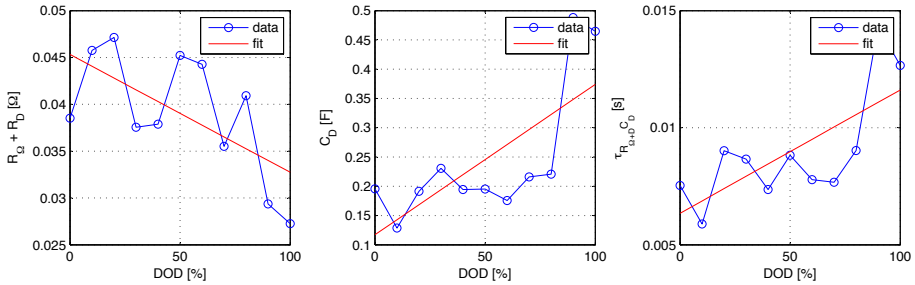


Figure 5.21: Diffusion parameters R_D, C_D and associated time constant τ_{RC} behaviour for different degrees of discharge. Large measurement variances make a reverse deduction to the state of charge difficult. The trend shows decreasing R_D, increasing C_D and increasing τ_{RC} for higher degrees of discharge.

In truth, R_D also contains the ohmic resistance R_Ω. The sharp voltage recovery jump is hidden behind a transient from relay bouncing. If transistors were used as switches, the settling times in the nanosecond scale would be better suited for a separate measurement of R_Ω. A simultaneous measurement of R_Ω and R_D would still be problematic due to maximum sampling speed required for R_Ω measurement leaving no space for enough subsequent samples which are needed to determine R_D.

5.2.1.4 Concentration Overpotential Parameters

In contrast to the previously discussed diffusion overpotential parameters, the concentration overpotential is a comparably slow process with time constants in the seconds range. Therefore, the calculation is conducted at the low sampling rate which is used to capture the whole discharge process. Figure 5.24 shows the results of the calculation. R_C ranges from $15m\Omega$ through $158m\Omega$ while steadily increasing and precisely measurable. C_C ranges from $715F$ through $100F$ while trending downwards, however not as steadily as R_C. Multiplied, they result in time constants from $7.3s$ through $18.2s$.

It is basically possible to determine these parameters while the battery voltage recovers from a current jump or while the current is still on. Figure 5.23 shows the estimation process while discharging. While trending similarly, all three values are higher. This is because the state of charge decreases while still measuring, resulting in larger voltage drops. Hence, a measurement during a recovery period with a constant SoC is advised.

5.2.1.5 Nyquist Plot

The results obtained can also be presented in a Nyquist Plot, which is shown in figure 5.25. Visible are two overpotential RC elements of very different time constants which vary for different degrees of discharge. For very high frequencies, this plot approaches 0Ω, as the ohmic resistance could not be obtained seperately from the diffusion resistance. These plots need to be compared to a real EIS to rate the accuracy.

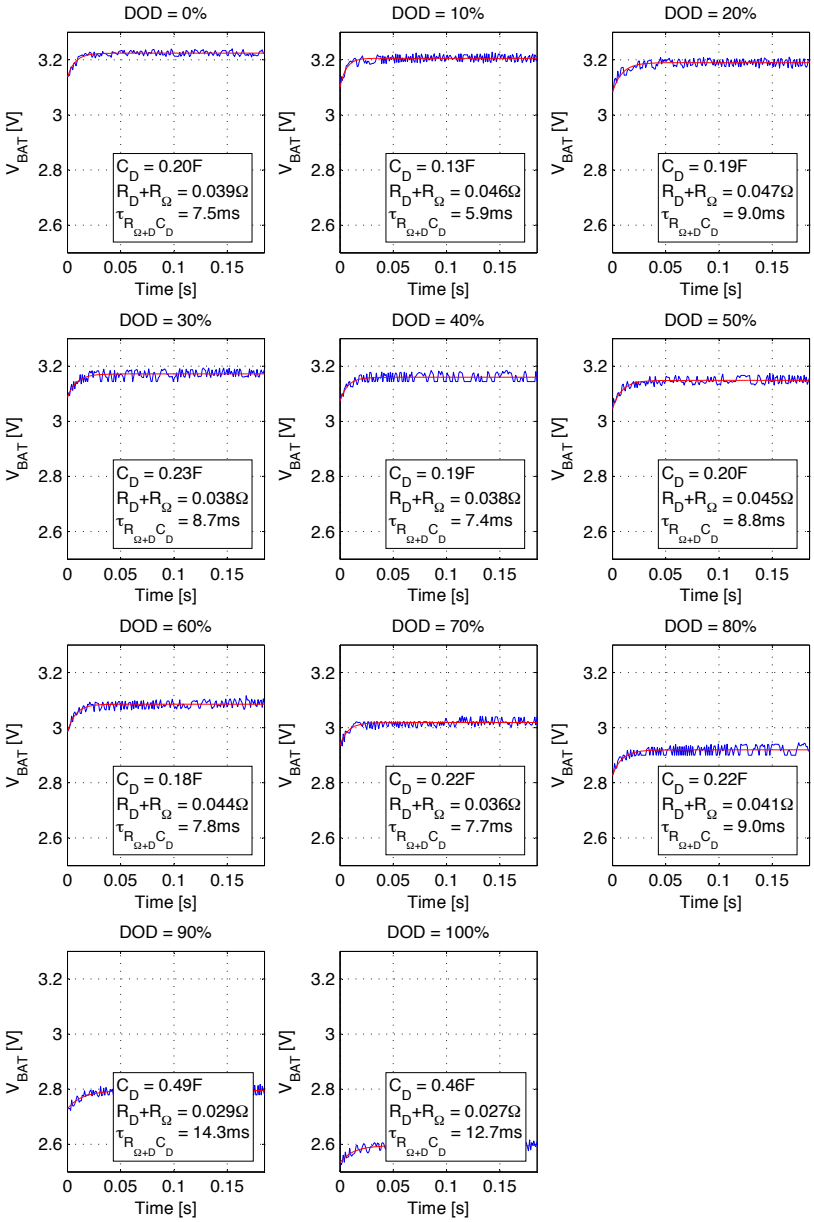


Figure 5.22: Diffusion process transients for different degrees of discharge. Diffusion happens relatively quickly, requires a faster sampling and comes along with more noise. N=185, $\Delta T = 1ms$.

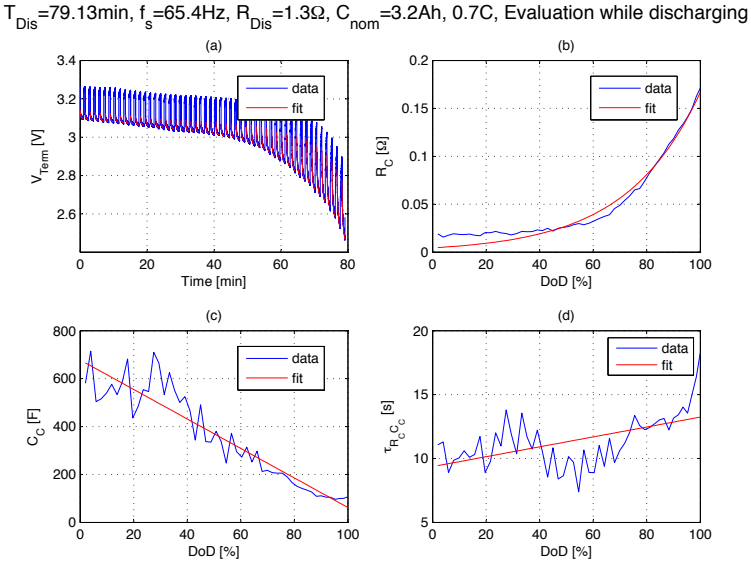


Figure 5.23: High discharge rate Concentration Overpotential Parameter Estimation for different degrees of discharge, estimated during recovery phases.

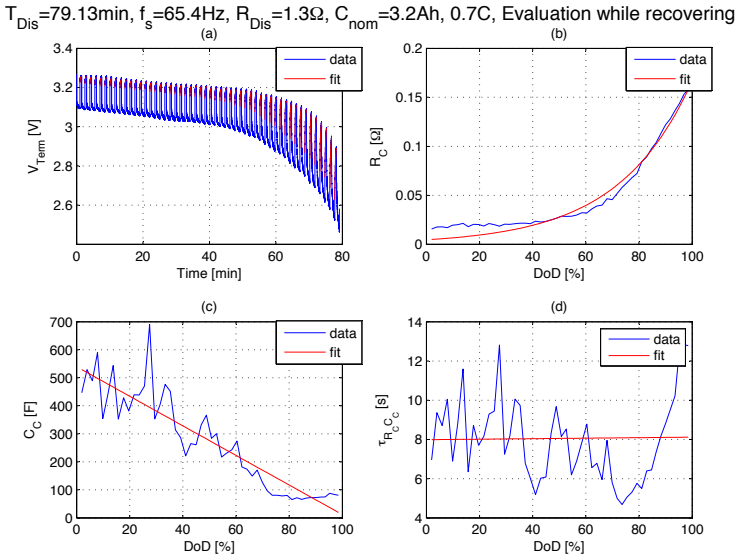


Figure 5.24: High discharge rate Concentration Overpotential Parameter Estimation for different degrees of discharge, estimated during discharging phases.

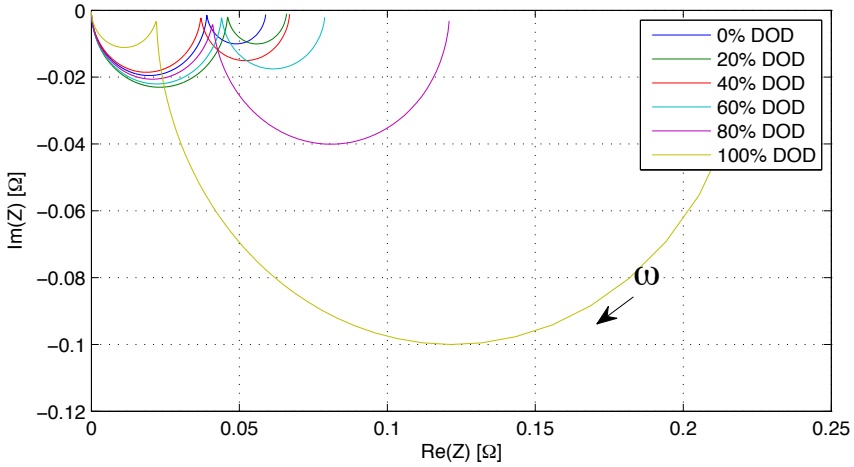


Figure 5.25: Nyquist Plot of High Discharge Unamplified Measurement Test Results for frequencies from $1mHz$ to $1kHz$.

5.2.2 Medium Discharge Rate Unamplified Measurement

5.2.2.1 Setup

The discharge current is reduced to a rate of 0.2C($\approx 650mA/2W$) with 10-seconds recovery periods after each 30 seconds of discharge and a slightly different test setup. This test is using the on-PCB balancing resistor and makes no use of the relay from figure 5.19 but uses the transistor as a switch. The measurement is distorted by a significant voltage drop across the thin PCB lines, which have a resistance of approximately 0.3Ω. The discharge test ran for 269 minutes while taking samples at a rate of f_s = 18.42Hz. This test also does not consider the ohmic resistance to be a part of the diffusion resistance, as has been done in the high discharge setup, but considers the diffusion resistance to be part of the ohmic resistance, to see if the results are more prone to measurement noise.

5.2.2.2 Capacity

First of all, a discharge test is conducted. Results are shown in figure 5.26. Of course, the typically flat trend at high SoC levels is visible (a). For example, the initial voltage of 3.25V drops to 3.10V only after 210 min, which corresponds to a DoD of 80%. While the SoC estimation using a common 10-bit ADC resolution would limit the SoC resolution to about 2.6% in that area, a 12-bit ADC can achieve a 0.65% resolution. The balancing current (b) is proportional to the terminal voltage. The depth of discharge reveals the age of the battery and the capacity loss involved. At this stage of development, the current supply of the whole board was 110mA and thus not negligible. Together with the recorded

maximum DoD of 2.12Ah, the total DoD was 2.61Ah, which means a 18.34% loss of the initial capacity.

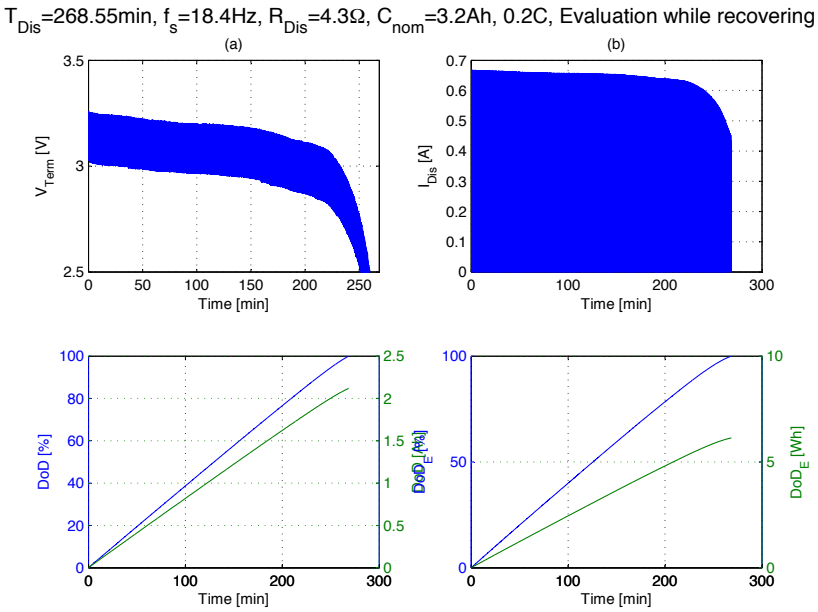


Figure 5.26: Discharge at 0.2C rate. More capacity is available compared to the 0.7C rate.

5.2.2.3 Ohmic Resistance Parameter

Next, the ohmic resistance is measured. Figure 5.27 shows the calculated ohmic inner resistance R_Ω. Ranging from $R_{\Omega,min} = 298m\Omega$ to $R_{\Omega,max} = 326m\Omega$, the ohmic resistance of the connectors clearly overtops the cell resistance, which is confirmed by a multimeter measurement of the connector resistance of $0.2 - 0.3\Omega$. This constant value could be determined by a precise low resistance measuring tool and be subtracted for a near-perfect estimation of the inner resistance. From this data set an increasing trend of R_Ω can be obtained, as figure 5.27 illustrates. The best linear fit reveals an increased ohmic resistance of $6m\Omega$.

5.2.2.4 Diffusion Overpotential Parameters

Diffusion Overpotential Parameters are skipped in this test as the lower sampling rate required for lower discharge rates is too low to resolve the diffusion process. Thus, the diffusion resistance is included in the ohmic resistance and the diffusion capacitance is not determined at all. Concentration Overpotential Parameters, on the other side, can still be obtained. The results are presented next.

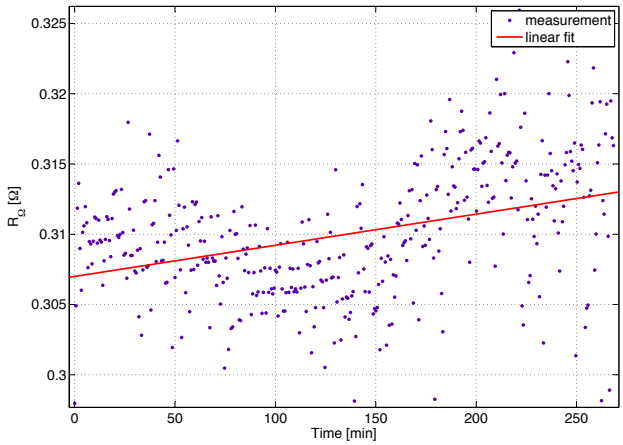


Figure 5.27: Medium discharge rate estimation of R_Ω. Within the given range, the variability of this parameter is pretty high. The best linear fit shows an increase of the inner resistance of $6m\Omega$.

5.2.2.5 Concentration Overpotential Parameters

As expressed in figure 5.28, both R_C and C_C show the same trend as in the high discharge tests (figure 5.24). However, both R_C and C_C tend to be smaller and ranges from $10m\Omega$ at 0% DoD to $50m\Omega$ at 80% DoD, $73m\Omega$ at 90%, $85m\Omega$ at 95% and then to increase rapidly to $212m\Omega$ at 100%.

C_C shows a decreasing trend from $310F$ at 0% DoD down to $24F$ at 100% DoD with a lot of variance.

Due to the constant trend of R_D and it's independance from the connector resistance it seems to be a better choice to rely upon for SoC determination rather than the ohmic resistance, which is very prone to fluctuation and dependant on the connector resistance, however the dependance on the discharge rate must be kept in mind.

5.2.2.6 Nyquist Plot

Figure 5.29 presents the results of the medium discharge rate unamplified measurement in a Nyquist Plot. Compared to the high discharge setup, the smaller half-circle from the diffusion overpotential is missing and a DC-Offset of 0.3Ω, introduced by the PCB wire resistance, can be observed.

5.2.3 Low Discharge Rate Amplified Measurement

When it comes to low discharge currents in the range of a C/20 rate or less, the voltage drop is too low to measure it unamplified. In the Formula SAE car, for instance, a 128Ah

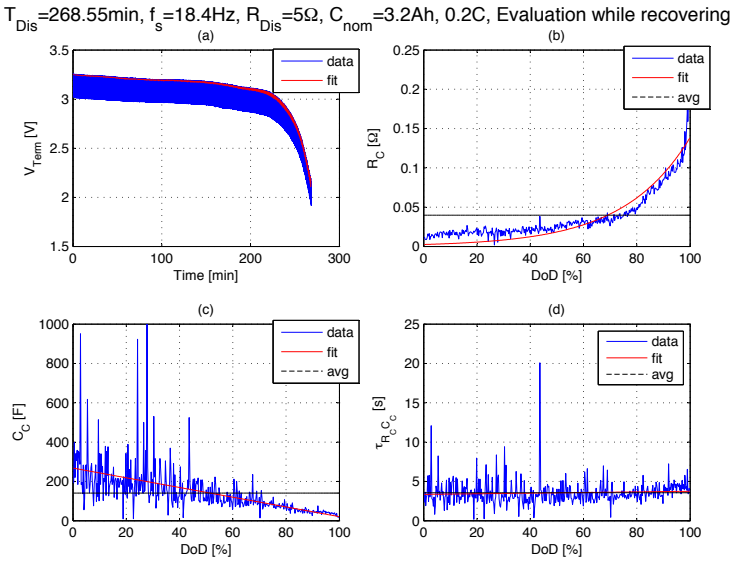


Figure 5.28: Concentration Overpotential Parameter Estimation for different degrees of discharge, estimated during recover phases, at a discharge rate of 0.2C.

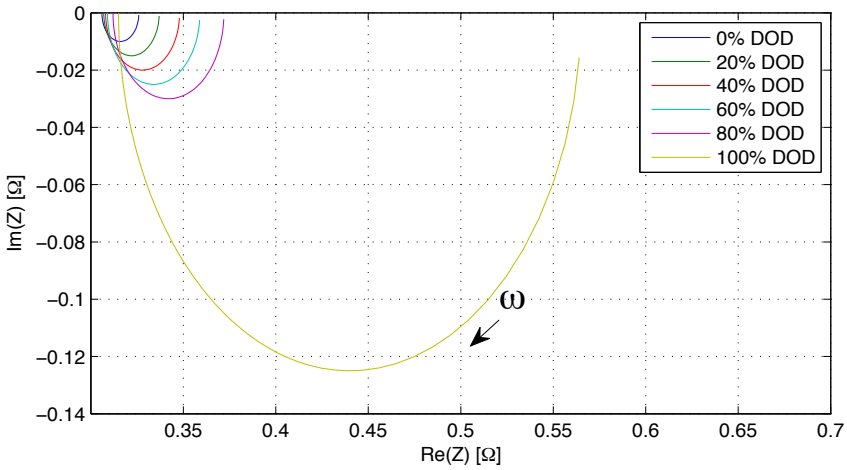


Figure 5.29: Nyquist Plot of Medium Discharge Unamplified Measurement Test Results for frequencies from 1*mHz* to 1*kHz*.

battery pack with a block resistance of $500\mu\Omega$ is used. To achieve a suitable voltage drop of $8mV$ in magnitude (using 3 bits of accuracy), a current jump of $16A$ needs to be applied, conducting up to $64W$ of heat for at least 30 seconds. This is not a viable option as not only it would require a massive radiator but would also drain the battery too much. Hence, the amplifier circuit which has been designed (see section 4.9.2) is used in combination with the balancing circuit as the voltage dropper, which exists anyway. When turning on the balancing current of $200mA$, the voltage drops by $100\mu V$. An amplification factor of

$$A = 500 \tag{5.16}$$

is used to achieve an output amplitude of $50mV$, which is applied to the ADC. As this amplitude is then referenced to ground rather than to the battery voltage, there is no more need for a voltage divider in front of the ADC. The internal voltage reference of the Microcontroller is $1.00V$ and therefore the signal can be applied directly, gaining another two bits of accuracy (a 1:4 voltage divider assumed), ending up with a quantizing accuracy of 7.7 bits for state of charge levels greater than 20%. Below these levels the voltage drop magnitude increases and with a headroom of $950mV$, there is still enough space to amplify these without clipping. Also, at the amplification level of $A = 54dB$, it is ensured that the op amp is far from reaching saturation, which would occur near it's open loop gain of $A_0 = 115dB$.

The Sample and Hold circuit had a measured droop rate of $5\frac{mV}{h}$ which equals to $1.4\frac{\mu V}{s}$ and is even better than the calculated value of $9.6\frac{\mu V}{s}$. The amplifier specifications have been successfully validated for an amplification factor of $A = 500$ and sample voltage drops have been successfully recorded according to the setup described in figure 5.30.

The discharge rate used in the balancing circuit of $C/640$ would take more than 26 days to discharge the battery and did not allow a complete automatic discharge test for time reasons within this work. A half-automatic discharge test with quick discharges to a coarse grid of SoC levels and measurements in between has not been conducted due to the lack of appropriate discharge equipment and sufficiently tested automatic discharge routines which gives the chance for an extensive examination to another work.

5.2.4 Conclusions

The last part of the inner parameter estimation section concludes the results. After all the tests conducted, it can be stated that time-domain measurements are suitable and provide with the expected results:

- Measurements of capacity work reliably in the time domain.
- Measurements of the ohmic resistance R_Ω work, but their accuracy is strongly dependant from very high sampling rates, to not falsely include parts of the voltage drop introduced by the diffusion overpotential in the ohmic resistance. High sampling rates come along with a high clock speed, which linearly increases the re-

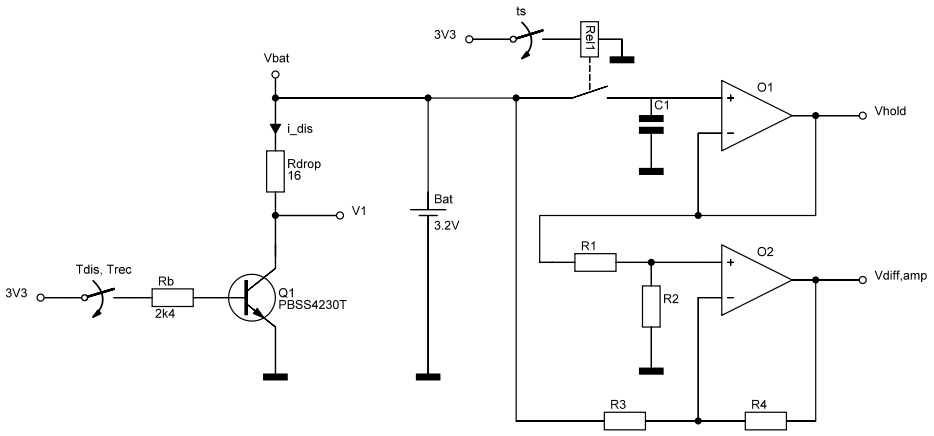


Figure 5.30: Low discharge rate voltage drop setup. The battery is discharged over R_{DROP} with the discharge current i_{dis} for a period of t_{dis}, followed by a recovery phase of t_{rec} and then repeated. During all the time the battery voltage Vbat is captured and later used to calculate the inner parameters of the battery. The potential V_{Rel} is used to calculate i_{dis} and track the degree of discharge.

quired power. The direct usage of the ohmic resistance for SoC determination is problematic.

- Measurements of the diffusion overpotential parameters R_D and C_D work at slightly higher but still reasonable sampling rates. An automatic measurement is advised with transistors as switches only, as relais come with a large settling time and bouncing can make the triggering complicated. Though in the trend, R_D decreases and C_D increases, both parameters are not usable for a direct estimation of the SoC.

- Measurements of the concentration overpotential R_C and C_C work best. Not only can they work at very low sampling rates, they are also pretty invariant to shifts in the start point of measurement, as the process is so slow that the diffusion overpotential does not interfere with the measurement any more. Parameter measurements show a very good trend, especially R_C is definitely a very good candidate for a direct SoC estimation.

- Given the choice between a measurement during discharge or recovery, the latter option should be preferred.

- If the proposed low droop low discharge rate precision amplifier is used, very little discharge test currents of smaller than a C/640 rate can be used while still achieving highly accurate results, making that method suitable for very large battery packs of more than 100Ah and dropping the drain from the battery to an absolute minimum.
- Nyquist Plots created from these parameters still need to be compared to the results of an EIS to prove their accuracy.
- Models for an accurate SoC and SoH determination, e.g. using Kalman filters, need to be derived in a further work. More training data for different discharge rates, sampling frequencies, required sampling accuracies and different ambient temperatures are a prerequisite for that endeavour. Relevant parts of the hard- and firmware and discussions of the test procedures have been provided.

6 Conclusions

6.1 Results

Both technological hurdles addressed in this thesis,

1. the constraint of having to use external communication wires and
2. the limited ability to obtain inner parameters without external measurement devices,

could be clearly reduced with the proposed technology. It has been shown that powerline communication is a viable solution for dedicated communication wires by achieving a success rate of over 99.9% of correctly transmitted packets in the worst-case scenario of an electric vehicle under load. Inner cell parameters which until now could be obtained by external electrochemical impedance spectroscopy devices only can now be derived from time-domain measurement evaluations on an industry-standard microcontroller.

6.2 Future Research

Subject of future research could be the development of a model to accurately deduct secondary inner parameters from the primary inner EEEC parameters given by the technology developed. Especially the determination of State of Charge and State of Health without prior knowledge of the cell and without relying on external circuitry as is needed for coulomb-counting, for example, could be a valuable benefit for the user convenience. Large amounts of training data of different cells from different manufacturers, of a different age, tested at different ambient temperatures are required to feed these models.

Intelligent battery packs capable of communicating with a charging station can help establish a grid of Multi-Voltage-DC-Quick-Charging-Stations as a temporary technology where electric vehicle manufacturers do not agree on a standardized battery voltage. The battery pack could instruct the charging station which voltage and charging current is required and the charging station can adapt to its needs.

As one charging station serves many customers, it would be more economic to put the chargers into the charging stations rather than into each single electric vehicle. That way, the high weight of a quick charger could be saved for each car. Even for the customer it would be interesting, since currently, batteries are no longer the limiting factor of a quick recharge.

Chargers, on the other hand, are still confining a quick recharge. High power chargers come along with high material costs and thus are expensive. Public charging stations

featuring ultra-fast chargers would break even a lot quicker than privately owned ones and as fast public chargers allow serving even more customers per day this would pay off for public stations rather than for private users.

No matter which road is taken, a strong foundation has been established which marks a new era of individual transportation as electric and hopefully, with this work, a small contribution to that success has been made.

List of Figures

List of Tables

Bibliography

D. Andrea. *Battery Management Systems for Large Lithium Ion Battery Packs*. Power engineering. Artech House, 2010. ISBN 9781608071043. URL http://books.google.com.au/books?id=o-QpFOROPTcC.

D.I.R. Benger. *Elektrochemische Impedanzspektroskopie zur Ermittlung der Parameter für ein Ersatzschaltbild elektrochemischer Speicher (Versuchsanleitung)*. Technical Report, Technische Universität Clausthal, 2007. URL http://www.iee.tu-clausthal.de/fileadmin/downloads/Praktikum/Fachpraktikum_V2_Skript.pdf.

B. Bhangu, P. Bentley, D. Stone, and C. Bingham. Nonlinear observers for predicting state-of-charge and state-of-health of lead-acid batteries for hybrid-electric vehicles. In *Vehicular Technology, IEEE Transactions on*, 54(3), pp. 783–794, 2005.

E. Biglieri. Coding and modulation for a horrible channel. In *Communications Magazine, IEEE*, 41(5), pp. 92 – 98, may 2003. ISSN 0163-6804. doi:10.1109/MCOM.2003.1200107.

S. Cheng, J. Zhang, M. Zhao, and C. Cao. Electrochemical impedance spectroscopy study of Ni/MH batteries. In *Journal of Alloys and Compounds*, 293â€“295(0), pp. 814 – 820, 1999. ISSN 0925-8388. doi:10.1016/S0925-8388(99)00363-1. URL http://www.sciencedirect.com/science/article/pii/S0925838899003631.

D. COMSOL, P. Updates, C.M. Books, S. Chart, C.S. Chart, C. Multiphysics, R. Module, M. Module, H.T. Module, S.M. Module et al.. In Electrochemical impedance spectroscopy of a lifepo4/li half-cell.

R. Dell, D. Rand, and R.S. of Chemistry (Great Britain). *Understanding Batteries*. Royal Society of Chemistry paperbacks. Royal Society of Chemistry, 2001. ISBN 9780854046058.

D. Doerffel and S.A. Sharkh. A critical review of using the Peukert equation for determining the remaining capacity of lead-acid and lithium-ion batteries. In *Journal of Power Sources*, 155(2), pp. 395 – 400, 2006. ISSN 0378-7753. doi:10.1016/j.jpowsour.2005.04.030. URL http://www.sciencedirect.com/science/article/pii/S0378775305007093.

K. Dostert. *Powerline-Kommunikation*, May 2012. CTAN: http://www.net-im-web.de/pdf/Dostert.pdf.

S. Galli and O. Logvinov. Recent developments in the standardization of power line communications within the ieee. In *Communications Magazine, IEEE*, 46(7), pp. 64–71, 2008.

O. Gérard, J.N. Patillon, and F. d'Alché Buc. Neural network adaptive modeling of battery discharge behavior. In W. Gerstner, A. Germond, M. Hasler, and J.D. Nicoud (eds.), *Artificial Neural Networks — ICANN'97*, volume 1327 of *Lecture Notes in Computer Science*, pp. 1095–1100. Springer Berlin Heidelberg, 1997. ISBN 978-3-540-63631-1. doi:10.1007/BFb0020299. URL http://dx.doi.org/10.1007/BFb0020299.

S. Grewal and D. Grant. A novel technique for modelling the state of charge of lithium ion batteries using artificial neural networks. In *Telecommunications Energy Conference, 2001. INTELEC 2001. Twenty-Third International*, pp. 174–179. Oct. ISSN 0537-9989. doi:10.1049/cp:20010596.

A. Jossen. Fundamentals of battery dynamics. In *Journal of Power Sources*, 154(2), pp. 530 – 538, 2006a. ISSN 0378-7753. doi:10.1016/j.jpowsour.2005.10.041. URL http://www.sciencedirect.com/science/article/pii/S0378775305014321. <ce:title>Selected papers from the Ninth Ulm Electrochemical Days</ce:title>.

A. Jossen. *Moderne Akkumulatoren richtig einsetzen*. Inge Reichardt Verlag, Untermeitingen, 2006b. ISBN 3939359114.

M. Jüstel, A. Schwinger, B. Friedrich, and M. Binnewies. Synthesis of lifepo4 by ultrasonic and nozzle spray pyrolysis. In *Zeitschrift für Physikalische Chemie*, 226(2), pp. 177–183, 2012.

L. Liao, P. Zuo, Y. Ma, X. Chen, Y. An, Y. Gao, and G. Yin. Effects of temperature on charge/discharge behaviors of LiFePO4 cathode for Li-ion batteries. In *Electrochimica Acta*, 60(0), pp. 269 – 273, 2012. ISSN 0013-4686. doi:10.1016/j.electacta.2011.11.041. URL http://www.sciencedirect.com/science/article/pii/S0013468611017129.

X.Z. Liao, Z.F. Ma, Y.S. He, X.M. Zhang, L. Wang, and Y. Jiang. Electrochemical behavior of lifepo4/ c cathode material for rechargeable lithium batteries. In *Journal of the Electrochemical Society*, 152(10), pp. A1969–A1973, 2005.

Y. Maryanka. Voice, music, video and data transmission over direct current wires. March 10 1998. US Patent 5,727,025.

Y. Maryanka. Signaling over noisy channels. March 7 2006. US Patent 7,010,050.

S.W. Moore and P.J. Schneider. A review of cell equalization methods for lithium ion and lithium polymer battery systems. In *SAE Publication*, pp. 01–0959, 2001.

K. Nishijima, H. Sakamoto, and K. Harada. A pwm controlled simple and high performance battery balancing system. In *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, volume 1, pp. 517–520. IEEE, 2000.

A. Padhi, K. Nanjundaswamy, and J.B.d. Goodenough. Phospho-olivines as positive-electrode materials for rechargeable lithium batteries. In *Journal of the Electrochemical Society*, 144(4), pp. 1188–1194, 1997.

W. Peukert. Über die abhängigkeit der kapazität von der entladestromstärke bei bleiakkumulatoren. In *Elektrotechnische Zeitschrift (ETZ). 18*, pp. 287–288, 1897.

G.L. Plett. Extended Kalman filtering for battery management systems of LiPB-based HEV battery packs: Part 3. State and parameter estimation. In *Journal of Power Sources*, 134(2), pp. 277 – 292, 2004. ISSN 0378-7753. doi:10.1016/j.jpowsour.2004.02.033. URL http://www.sciencedirect.com/science/article/pii/S0378775304003611.

V. Pop. *Battery Management Systems: Accurate State-Of-Charge Indication for Battery Powered Applications*. Philips Research Book Series. Springer Science + Business Media B.V, 2008. ISBN 9781402069451.

M.A. Roscher and D.U. Sauer. In Dynamic electric behavior and open-circuit-voltage modeling of LiFePO4-based lithium ion secondary batteries", journal = "Journal of Power Sources, 196(1), pp. 331 – 336, 2011. ISSN 0378-7753. doi:10.1016/j.jpowsour.2010.06.098. URL http://www.sciencedirect.com/science/article/pii/S0378775310010852.

A.J. Salkind, C. Fennie, P. Singh, T. Atwater, and D.E. Reisner. Determination of state-of-charge and state-of-health of batteries by fuzzy logic methodology. In *Journal of Power Sources*, 80(1â€“2), pp. 293 – 300, 1999. ISSN 0378-7753. doi:10.1016/S0378-7753(99)00079-8. URL http://www.sciencedirect.com/science/article/pii/S0378775399000798.

U. Tietze, C. Schenk, and C. Schenk. *Halbleiter-Schaltungstechnik*. Springer, 2002. ISBN 9783540428497. URL http://books.google.com.au/books?id=h6A0HyamoTIC.

D.H. Wenzl. *Ersatzschaltbilder und Modelle. Die unterschiedlichen Auswirkungen auf die elektrischen Eigenschaften der Komponenten der Batterie beim Laden, Entladen und beim Altern.* Technical Report, Technische Universität Clausthal, 2006. URL http://www.iee.tu-clausthal.de/fileadmin/downloads/Scripte/W8816_kapitel5.pdf.