CPU sample mid sem solution

Step	PC	Command	Accu (after)
0	0x00	10 10 LOAD-I	0x10
1	0x02	13 FF ADD-I	0x0F
2	0x04	03 01 ADD-M	0x1F
3	0x06	13 01 ADD-I	0x20
4	0x08	17 FD BRZ (PC is 0x09 at branching)	0x20
5	0x06	13 01 ADD-I	0x21
6	0x08	17 FD BRZ	0x21

The first 4 steps (0-3) should be relatively easy. For this CPU the most significant hex value of the OP code tells you if you are using a constant (1) or memory (0). The least significant HEX value tells you the operation you are performing at the accumulator. When we get to the next step there are some things to be careful about. First the op code is 7 which has a check that goes into a 3 input and gate. This gate waits for the branch pulse, checks to see if the op code is 7 and then also looks at the OR gate. The accumulator is not 0 but the 5^{th} bit from the op code is 1 so all the conditions are true for branching to occur. This changes the multiplexer to pass through the ADDRESS register instead of a 1, so the next time the PC is pulsed means it would add the contents of ADDRESS to its current value. The other thing to note is how the PC works in this PC. Since the RAM is 8 bit output and both the registers use 8 bit values. Therefore to load our initial conditions we need to first load the op code value, then increment the PC to look at the next address (containing the data/address value) and then load that value into the ADDRESS register. Therefore the PC currently for step 5 will actually be 0x09 not 0x08. Therefore the value that gets added to 0xFD is 0x09 not 0x08 with a final result of 0x06 which gets loaded back into the PC. At this point we are in an infinite loop that increments by one on each loop.